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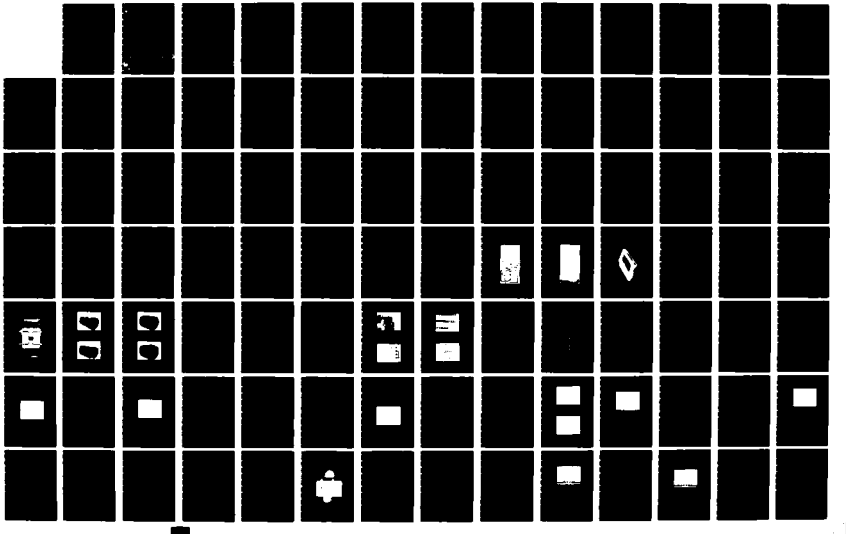

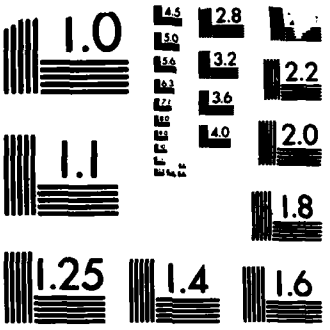

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SINGLE CIRCUIT BOARD IMPLEMENTATION OF A DIGITALLY COMPENSATED SAW OSCILLATOR (DCSO)

THESIS

AFIT/GE/EE/83D-44 Jerry W. McGuire
Capt USAF

DEPARTMENT OF THE AIR FORCE
AIR UNIVERSITY (ATC)
AIR FORCE INSTITUTE OF TECHNOLOGY

Wright-Patterson Air Force Base, Ohio

AFIT/GE/EE/83D-44

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THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
in Partial Fulfillment of the
Requirements for the Degree of
Master of Science in Electrical Engineering

by

Jerry W. McGuire, B.S.
Capt USAF
Graduate Electrical Engineering

December 1983

Preface

Through this project a design for a Digitally Compensated SAW Oscillator (DCSO) was developed and implemented on a single circuit board. The AFIT IC, which is the heart of the design, did not function properly. Therefore, my work was halted after testing several of the subcircuits and assembling the components on the final version of the circuit board.

During my thesis work, the efforts of several people helped to make this a successful learning experience for me. My appreciation goes out to Larry Calahan for his assistance in circuit board fabrication, and to Carl Shorte and his craftsmen at the AFIT machine shop for building the DCSO package. A special thanks is due to Andy Slobodnik for allowing me to use his ideas in laying out the DCSO circuit, and to Roger Colvin for his exceptional guidance and insight into the problems encountered during this thesis effort. Also due a special thanks is my wife, Sue, for her patience and understanding.

Jerry W. McGuire

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Abstract

A circuit, using standard "off-the-shelf" components, for digital temperature compensation of a SAW oscillator was designed. This circuit was implemented on a single circuit board. A crucial component of the circuit, the AFIT IC, designed by four previous AFIT students and fabricated by NCR, failed to operate at a required frequency of 37 MHz. This caused an early halt to the project; however, several parts of the design were tested individually with good results.

The portion of the circuit consisting of the D/A converter, op amp, and phase shifter was tested. For various addresses programmed on the D/A converter inputs, which simulated the output from the two EPROMs, a total phase shift of 107 degrees was obtained from the phase shift circuit.

The thermometer and clock paths of the SAW device were made to oscillate at their respective resonant frequencies by introducing the proper amounts of phase shift and attenuation into the feedback loops. The thermometer and clock resonant frequencies were 309 MHz and 298 MHz respectively.

Testing of the SAW feedback loops in conjunction with the phase shifter circuit showed the clock loop frequency could be varied over a range of 210.7 KHz. The thermometer loop frequency had a slight variation of 7.6 KHz. Finally, the SAW clock loop produced an output power of +9 dBm.

SINGLE CIRCUIT BOARD IMPLEMENTATION OF A DIGITALLY COMPENSATED SAW OSCILLATOR

I. Introduction

Background (Ref. 12:2-3)

A surface acoustic wave (SAW) is a high frequency elastic wave that can be guided along the surface of a piezoelectric material. A simple SAW device is shown in Figure I-1. The elastic wave is launched at one end of the crystal by fields generated at interdigital transducers (IDT), and the energy of the wave is generally confined to within a few wavelengths of the surface (Ref. 17:581)

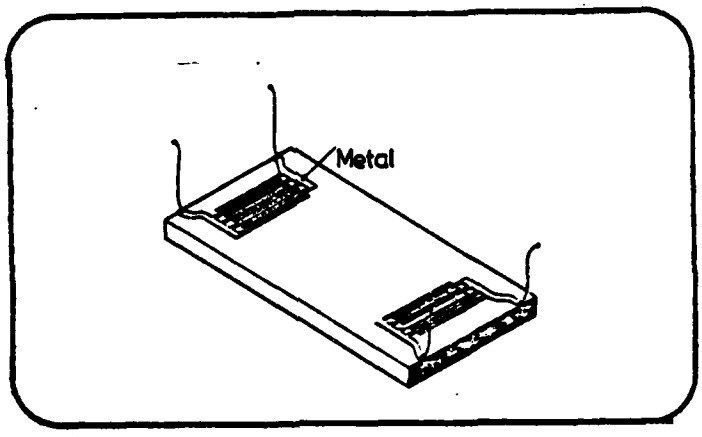


Fig. I-1 - Simple SAW Device (Ref. 12:3)

The most important property of SAW waves is their extremely low velocity which makes them ideal for long delay lines. Because of the low velocity, SAW waves also possess

extremely small wavelengths when compared with electromagnetic waves of the same frequency. SAW wave devices, when compared with electromagnetic devices, therefore offer dramatic reductions in size and weight. Also, the wave is easily accessible thus providing new flexibility in the creation of a variety of devices such as bandpass filters, oscillators, delay lines, dispersers, and convolvers. These devices are compatible with integrated circuit technology in that they can be fabricated on a crystal surface using standard lithographic techniques. This allows them to be mass produced at relatively low cost. Consequently, the device characteristics are easily reproduced, varying little from device to device.

The generation of precise frequencies by means of crystal controlled oscillators is an important electronics function and SAW devices have shown themselves to be a particularly cost effective implementation of this function. However, a problem associated with the generation of precise frequencies which is shared by both bulk and SAW devices is that of maintaining frequency stability over a wide range of temperatures. The inherent temperature sensitivity of the crystal element leads to a variation of the frequency of oscillation with temperature (Ref. 18:8). This frequency variation can be on the order of several hundred parts per million (ppm) over a temperature range of 100 degrees celcius.

Summary of Current Knowledge (Ref. 7:849-850)

Typically, two approaches to temperature stability of SAW oscillators are implemented. The crystal may be maintained at constant temperature through the use of an oven, but this technique requires relatively high power consumption, large space requirements, and has limited reliability due to oven failure associated with "ON-OFF" cycling.

Several electronic compensation techniques have been tried in which a voltage-controlled phase shift element in the oscillator feedback loop provides compensation by applying properly tailored temperature-dependent signals to the oscillator. These compensation methods can be broadly categorized into two types: analog and digital.

Most analog compensation techniques make use of an n-point resistor-thermistor network in which the component values are adjusted to produce the proper control voltage at n-different temperatures. The major drawback to this scheme is that in order to obtain accurate control over a wide temperature range, the number of degrees of freedom (i.e. circuit components) becomes unwieldy. R. G. Kinsman (1978) demonstrated a simple compensation technique using back-to-back varactor diodes to produce a quasi-parabolic phase variation which mirrored that of the SAW device. The problem with this technique is that the diodes must be carefully matched. This is a difficult task at best. Another technique, demonstrated by Browning and Lewis

(1978), used dual path delay lines to synthesize the cubic temperature behavior similar to that of AT-cut bulk wave devices, but this technique is limited to fairly short delay lines.

Digital temperature compensation, which provides a set of preprogrammed control voltages over fixed temperature intervals using Erasable Programmable Read Only Memories (EPROMs), has provided the most accurate control but requires rather sophisticated electronics.

A major problem with all of the temperature compensation techniques discussed thus far is that they all require the use of either thermistors or thermocouples attached to the crystal surface in order to measure the temperature change of the crystal. This is not the most accurate method of measuring temperature changes.

A. J. Slobodnik (1981) used a simple, effective means to digitally compensate for the temperature sensitivity of a SAW oscillator (Ref. 18:8). The key feature of this Digitally Compensated SAW Oscillator (DCSO) is the use of two criss-crossing delay paths on the same SAW substrate. A sketch of the overall DCSO system is shown in Figure I-2.

The first path is aligned with a SAW orientation having traditional low temperature sensitivity properties; that is, an orientation having at least one zero temperature coefficient of delay within the temperature range of interest. By means of oscillation around a feedback loop, this device provides the precise frequency (or clock) which

can be improved further with digital control. Ordinary SAW oscillators use only this single clock path. The second delay path, crossing over the first path, is aligned with a SAW orientation having a high temperature coefficient of delay and acts, through its frequency of oscillation, as a thermometer or temperature measuring device. This configuration minimizes contact and time constant problems with the result that extremely accurate temperature sensing is possible (Ref. 18:8).

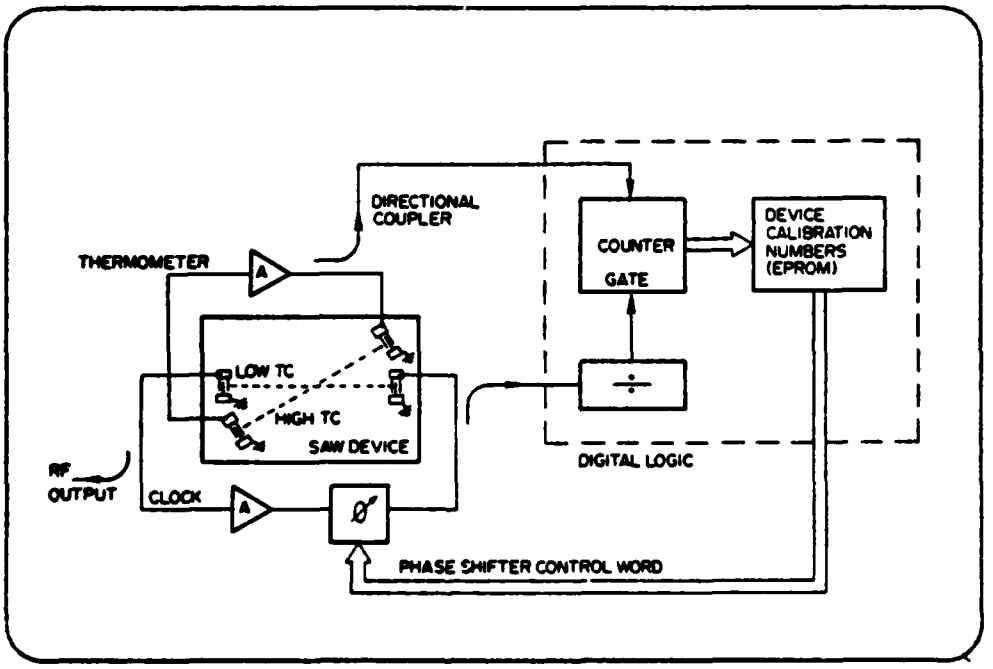


Fig. I-2 - Overall DCSO System (Ref. 18:9).

The output of a digital counter operating on the thermometer frequency provides a count which is a direct measure of temperature. This count is fed to a precalibrated EPROM. At each temperature, the phase shifter

control word necessary to maintain a stable clock frequency is applied by the EPROM to the electronically variable phase shifter via a digital-to-analog (D/A) converter. Since the clock frequency is always precisely maintained, it can be used to provide a constant duration gate signal to the counter. System convergence is assured due to the intentional difference in temperature coefficients of the two delay paths (Ref. 18:9).

The system is relatively simple. The clock frequency itself is directly available as an output; no further manipulation or frequency synthesis of the signal is required. Major advantages of this scheme include optimum temperature sensing, very fast warmup, and low cost (Ref. 18:9).

Objective

The DCSO has been proven to be an effective technique for reducing SAW oscillator temperature sensitivity. However, in order to take full advantage of the previously mentioned properties of this technique, several tasks remain.

The controller circuitry, which counts the thermometer frequency and derives the proper address for the phase shifter control word from the EPROM, has been designed using Complimentary Metal Oxide Semiconductor/Silicon on Saphire (CMOS/SOS) technology. However, a working chip has yet to be manufactured and tested. Once the controller circuit

chip (hereafter called the AFIT IC) has been manufactured by a contractor, it will be tested for proper operation.

The radio frequency (RF) electronics for the circuit are quite large. A single hybrid RF circuit will solve this problem. This RF circuit will contain amplifiers, directional couplers, a varactor phase shifter, and other appropriate components. Once this hybrid RF circuit is available, it will be integrated onto a single circuit board with the AFIT IC, a SAW device, and a single chip digital-to-analog (D/A) converter. This circuit board will be designed to be as small as possible.

Scope

This thesis project will involve building and testing the single circuit board DCSO using standard off-the-shelf components. Non-standard components to be used will be the AFIT IC chip and the SAW device. Specifications determined from the design analysis will be used in choosing the individual components to be used.

The 300 MHz SAW device, supplied by Rome Air Development Center, will have the matching inductors already installed and no re-design or fabrication of the basic SAW device will be done.

The AFIT IC chip was designed by a team of students in 1982, fabricated by NCR, tested, and a revised design was submitted to NCR. This revised design will be tested as part of this thesis.

Standards

The RF portion of the circuit requires a ground plane. This means that the entire back side of the board opposite the RF circuit will need a continuous metal surface. Only where components are connected to the board will there be bare areas where the metal, in this case copper, will be etched away. Also, the RF circuit must have 50-ohm transmission lines. Therefore, the lines must be maintained to a specified width. This width varies depending on the type of material used for the circuit board. For this project, the circuit board material will be a copper clad teflon/glass laminate known as 3M CuClad 250 GX. This material was designed specifically for microstrip applications with close tolerance requirements, and machining and drilling of this material is easily accomplished. For this particular material, a transmission line width of .174-in. (174 mils) is recommended by the manufacturer.

The transmission lines must be kept as short as possible and spacing between the lines should be at least 5 times the width of a single line. This reduces any cross-coupling effects due to the propagating high frequency signal. In some instances, it may be necessary to put these lines somewhat closer together because of space requirements on the circuit board. However, in those few instances, a thorough analysis of the cross-coupling effects will be performed and a sound engineering judgement made as to

whether these effects are significant.

All lines on the digital portion of the board must be at least .010-in. (10 mils) wide and spaced 10 mils apart. This is necessary because it is the lower limit for the process used to etch these lines. Also, since a ground plane is not necessary for the digital circuit, both sides of the board can be used for routing the lines to various components.

Approach

Standard circuit analysis techniques will be used in the analysis and design of the hybrid RF and digital circuitry for the DCSO system.

Design standards will be adhered to in the layout of the circuit board. After the circuit board has been fabricated, the components (chosen as a result of the design analysis) will be mounted and tested individually for proper operation. Once proper operation of the individual components is verified, the entire board will be placed in an oven and the temperature varied so that data can be acquired to determine the correct phase shifter control words to be programmed into the EPROMs.

After the EPROMs are programmed, the oven temperature will again be varied while the output frequency of the SAW device is monitored. The results of this test will be fully documented.

Sequence of Presentation

In Chapter II of this report, an overview of the overall DCSO circuit is given. Also, the design and analysis of major parts of the circuit, such as the RF portion and the phase shifter, are presented. This is followed by a detailed description of the circuit board design. Next, in Chapter III, procedures used to test several of the major components of the circuit are given. Finally, in Chapter IV, conclusions arrived at while working on this project and recommendations for further work are given.

The manufacturers' specifications for the components used in building the DCSO circuit are given in Appendix A. Raw data from several of the tests are listed in Appendices B, C, and D. The final appendix contains package drawings.

II. Design and Analysis

Circuit Overview

The overall circuit diagram for the DCSO is shown in Figure II-1. One Avantek UTO-524 microwave amplifier (MICamp) is used in the temperature sensing loop of the SAW device. This thermometer loop also contains an Anzac DS-109 two-way power divider which divides the output signal from the MICamp. Half of the signal is fed to the DCSO controller circuitry (AFIT IC) via a Pyrofilm PCA thin film chip attenuator, a Plessy SP8735B high speed divider, and a Motorola MC10124 quad TTL-to-MECL translator. The SP8735B high speed divider scales the thermometer loop frequency from 300 MHz down to 37.5 MHz which is in the operating range of the AFIT IC. A phase shifter control word, stored in the two Intel 2716 EPROMs, is accessed depending on the address applied by the AFIT IC address lines. The control word from the EPROMs is applied to a Burr Brown DAC85CQ-CBI-V digital-to-analog converter. The resulting output analog voltage from the digital-to-analog converter is amplified by an LM3900N operational amplifier (Op Amp). The resistor network chosen for the LM3900N Op Amp amplifies the voltage signal by a factor of three. The output of the LM3900N Op Amp circuit is applied to the phase shifter network containing two MSI HA1717 varactor diodes, two radio frequency chokes (RFC), three microwave capacitors, and a

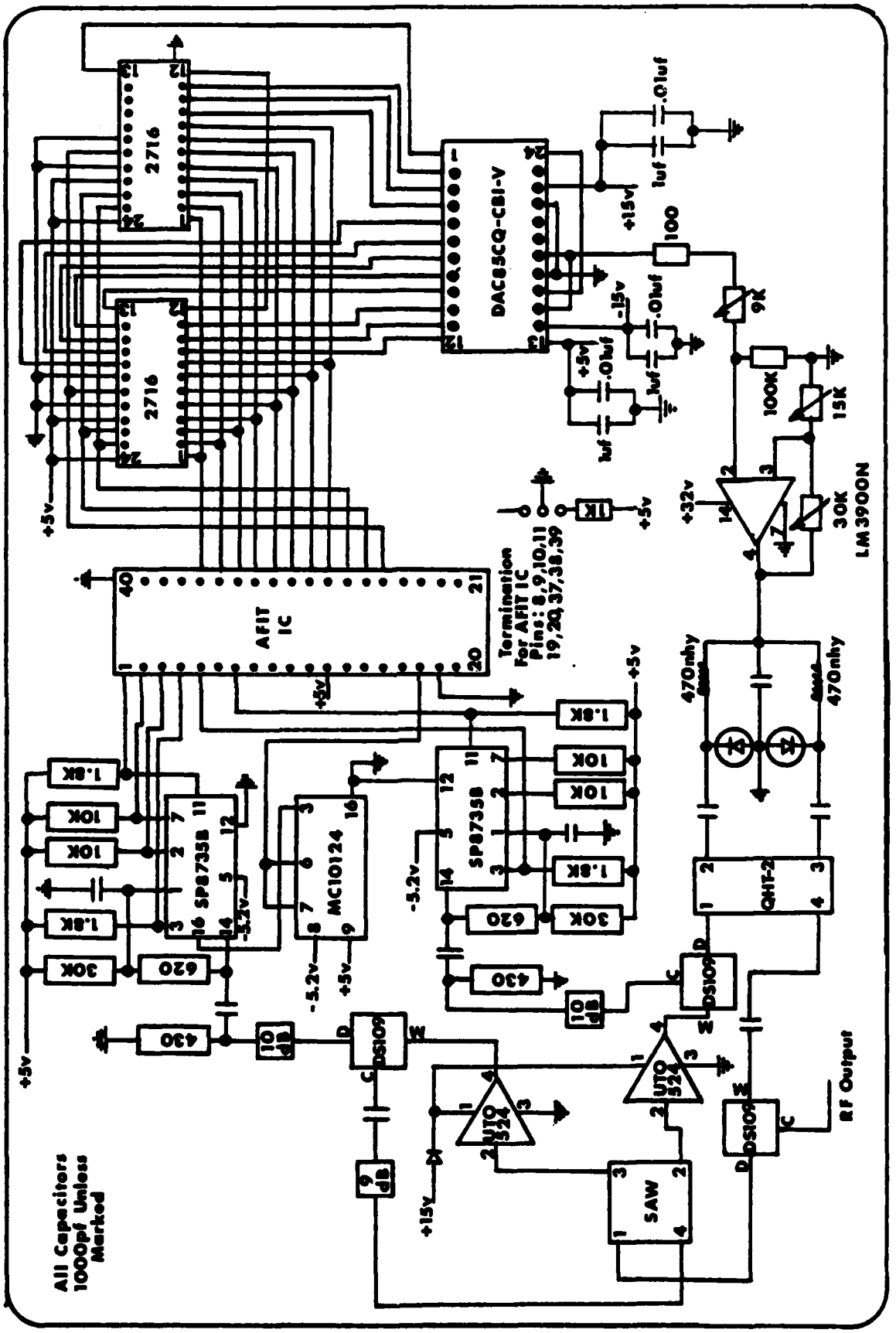


Fig. II-1. DCSO Circuit

Merrimac QHT-2 90 degree quadrature hybrid coupler. The second input to the phase shifter comes from the coupled output of the DCSO clock loop. This voltage is phase shifted by the phase shift circuitry to maintain a constant 300 MHz frequency over the desired temperature range. The DCSO clock loop also contains an Avantek UTO-524 MICamp. Two Anzac DS-109 two-way power dividers are used. One divider is used to couple the 300 MHz signal directly from the loop as an output. The other divider is used to couple half of the clock signal for the input to another Plessy SP8735B high speed divider which scales the clock frequency down to 37.5 MHz for the clock input to the AFIT IC. Specifications for major circuit components are discussed in Appendix A.

RF Circuit Design

The circuit diagram for the RF portion of the DCSO circuit is shown in Figure II-2. Although the phase shifter is included in the RF portion, its design is discussed separately in a later section.

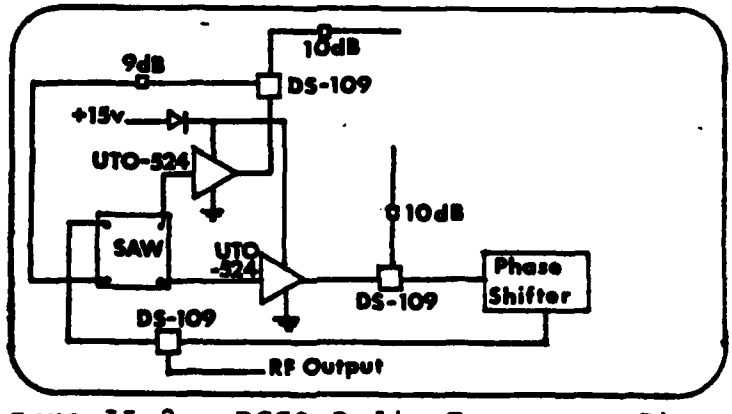


Figure II-2 - DCSO Radio Frequency Circuit.

Beginning with the DCSO clock loop, it is known that the Plessy high speed divider requires a clock input of 400-800 millivolts peak-to-peak (Ref. 14:174). If 800 mV peak-to-peak is taken as the desired input and the impedance of the transmission line is assumed to be 50 ohms, the root mean square (rms) voltage and power required can be calculated from:

$$V_{rms} = (V_p/1.414) = (0.4v/1.414) = 0.283\ v \qquad \text{Eq. II-1.}$$

$$P = (V_{rms})^2 / R = (0.283\ v)^2/50\ \text{ohms} = 1.6\ mW \qquad \text{Eq. II-2.}$$

Converting to dBm gives:

$$dBm = 10 \log (Power/0.001) =$$
$$10 \log (0.0016/0.001) = 2.04\ dBm \qquad \text{Eq. II-3.}$$

Now, assuming approximately 18 dB of loss across the SAW device, 5 dB of loss across the phase shifter, and 3.5 dB of loss across each of the two power dividers, it is realized that the amplifier must have at least 30 dB of gain. The Avantek UTO-524 MICamp has the necessary gain with a 1 dB gain compression of 14 dBm (25.12mW). For oscillation to occur, the losses around the closed loop must be less than the gain (i.e. gain > 1). This implies that the amplifier will go into saturation and, in this condition, it is not unreasonable to expect a saturated gain

of 16 dBm (39.81mW). From this, the power at the input to the attenuator is:

$$P = (39.81mW) \text{ antilog } (-3.5 \text{ dB}/10) =$$

$$17.78mW = 12.5 \text{ dBm} \qquad \text{Eq. II-4.}$$

Since only 1.6mW (2.05 dBm) is required for the Plessy clock input, a 10 dB attenuator is used to reduce the Plessy input signal power to 1.78mW (2.5 dBm). This is slightly more power than required but it should not adversly affect the operation of the Plessy circuit.

The power remaining at the input to the phase shifter is also 17.78mW (12.5 dBm) since the input power to the DS-109 is divided equally between the C and D output ports. The calculated loss across the phase shifter is 12.15mW, leaving 5.62mW (7.5 dBm) at the phase shifter output. The power at the RF output of the second DS-109 power divider is 2.51mW (4 dBm). Again, since the power is divided equally, the same power is present at the input to the SAW device clock path. The 18 dB insertion loss of the SAW device leaves 0.0398mW (-14 dBm) at the input to the MICamp, and the output power of the MICamp is:

$$0.0398 \text{ antilog } (30 \text{ dB}/10) = 39.8mW = 16 \text{ dBm as expected.}$$

The input power to the SAW device thermometer path should be approximately the same as the input power to the clock path. Considering the thermometer loop, the gain of the MICamp is again 30 dB with a 1 dB gain compression of

14 dBm. Assuming that this amplifier will also be saturated, the output power will be 39.81mW (16 dBm). The DS-109 will divide this power such that the power output at each of its ports is 17.78mW (12.5 dBm). A 10 dB attenuator is again required at the input to the Plessy high speed divider in order to drop the power to 1.78mW (2.5 dBm). As before, this is slightly more power than needed but no adverse effects on the Plessy circuit is expected. The output power at the C port of the power divider is 17.78mW (12.5 dBm) and, therefore, an 8.5 dB attenuator is needed in the thermometer feedback loop to reduce the SAW device input power to 2.51mW (4 dBm). Since attenuators of this value are not readily available, a 9 dB attenuator must be used instead. This lowers the input power to the SAW device thermometer path to 2.24mW (3.5 dBm). The power dissipated due to the 18 dB insertion loss of the SAW thermometer path is calculated as before with the result that the input power to the MICamp is 0.0355mW (-14.5 dBm) and the output power of the MICamp is:

0.0355 antilog (30 dB/10) = 35.5mW = 15.5 dBm.

This analysis shows a 30 dB MICamp gain is not enough for the thermometer loop. Instead, a gain of 30.5 dB is needed. This does not create a problem because the Avantek UTO-524 has a guaranteed minimum gain of 30 dB and the actual gain should be in excess of 30 dB.

Avantek UTO-524 MICamp. Since there is no cascading of amplifiers in the DCSO circuit, no special biasing network is required for the MICamps in the clock and thermometer loops. However, a silicon diode was added in series with the input d.c bias voltage line to provide reverse-voltage protection for the amplifiers. This causes an additional 0.6 volt decrease in input voltage which may be ignored, since the MICamp current drain is constant and the small drop in voltage should have no appreciable effect on the amplifiers' performance (Ref. 1:14).

Anzac DS-109 Power Divider. The DCSO circuit uses three DS-109 power dividers; one in the thermometer loop and two in the clock loop. In the power divider configuration, the summing junction is used as the signal input while the C and D ports provide the divided signal output. The DS-109 has eight leads, and all leads, except the sum, C, and D ports are tied to ground.

SAW Device. Tunable matching inductors are included in the SAW package and the assumed insertion loss includes any loss due to these inductors. Access to the inductors is provided by small holes drilled in the underside of the SAW case.

Digital Control Circuitry

In general, the digital control circuitry can be

thought of as the Plessy prescaler circuit, the TTL-to-MECL translator, the AFIT IC, and the Intel EPROMs. Each of these is discussed in the sections that follow.

Plessy SP8735B High Speed Divider. The DCSO prescaler circuit using the SP8735B is shown in Figure II-3. This is essentially the same circuit shown in Figure 5 on page 166 of the Plessy " Digital Integrated Circuits " book dated November 1979 and reproduced in Figure II-4 for comparison . The difference is that 1000 pf capacitors are used instead of 30 pf capacitors in both locations. The 1000 pf capacitors were used because they were readily available, and the Plessy application notes indicated that this would be adequate for the circuit. Also, a 430 ohm resistor to ground at the clock input is used instead of the 51 ohm resistor. The 430 ohm resistor provides better impedance matching than the 51 ohm resistor. Provisions have been made for adding the 2N5771 PNP emitter follower if more power is needed to drive the AFIT IC T-Chain input. According to the manufacturer, the 1000 pf UHF capacitor which couples the clock to the signal source, should be adequate. The clock input is gated by the ECL 10K input supplied by the Motorola MC10124 chip. The bias decoupling (pin 1) is connected to ground via a 1000 pf low inductance UHF capacitor as well. The SP8735B normally has an input amplitude operating range far greater than the specified 400-800 mV p-p. However, if the decoupling capacitor is not

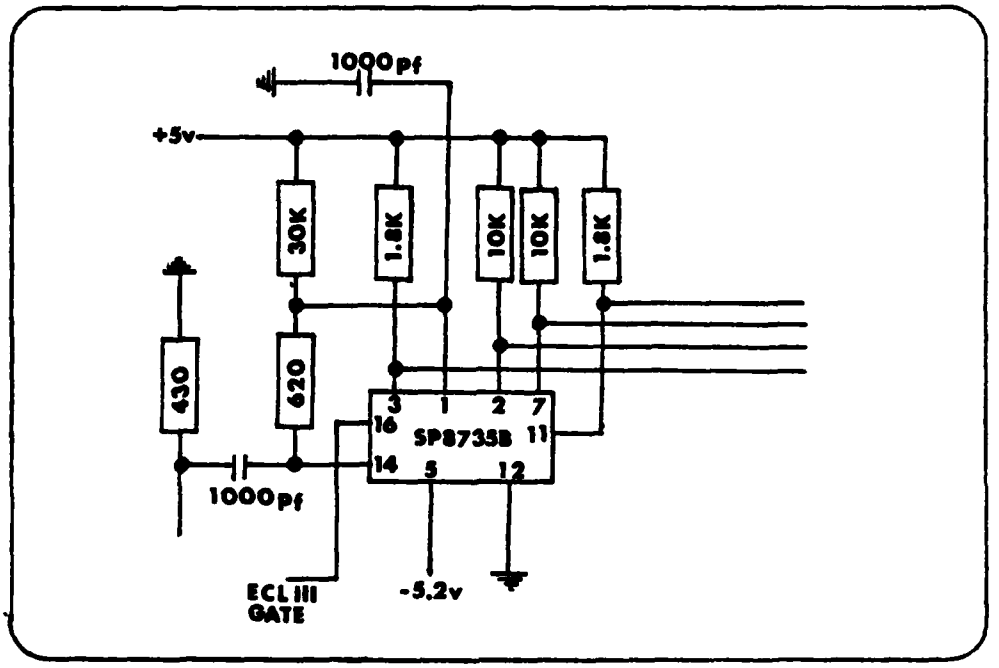


Fig. II-3 - DCSO Prescaler Circuit.

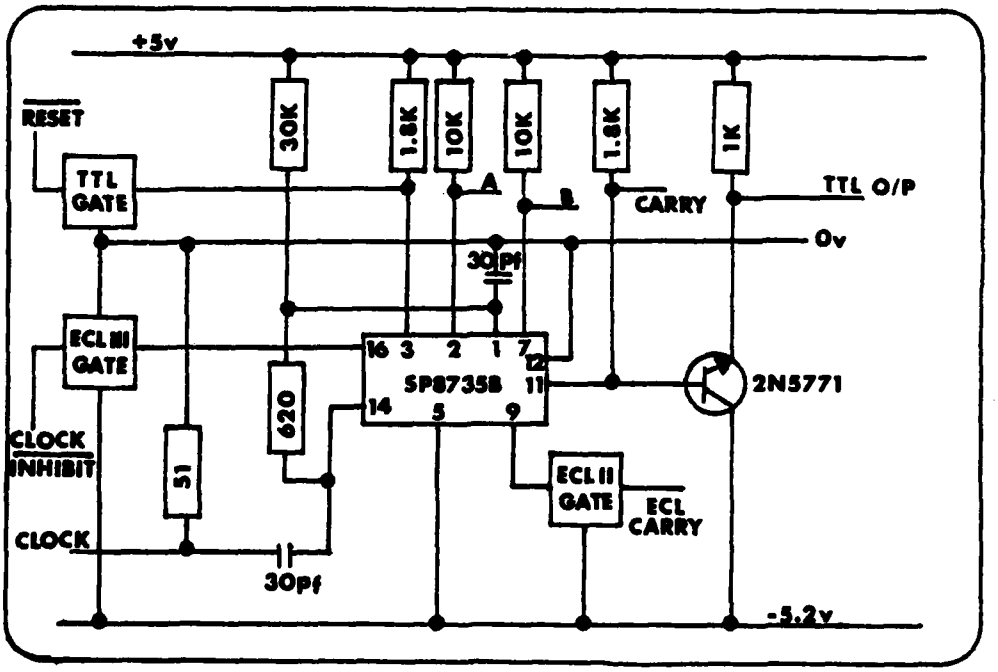


Fig. II-4 - Suggested Prescaler Circuit.

a UHF type, or it is connected to a ground point that has a significant impedance between the capacitor and the Vcc connection, then the input dynamic range will suffer and the maximum signal for correct operation will be reduced (Ref. 14:175).

The 30K ohm resistor connected between the positive power supply and pin 1 as well as the 620 ohm resistor connected between the clock input and pin 1 prevents the SP8735B from going into self-oscillation in the absence of an input signal (Ref. 14:175).

Motorola MC10124 TTL-to-MECL Translator. The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the Emitter Coupled Logic (ECL) section of digital systems. The device has Transistor Transistor Logic (TTL) compatible inputs, and ECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to an ECL low logic state and all inverting outputs to an ECL high logic state (Ref. 15:3-59).

As used in the DCSO circuit, the gate signal from the AFIT IC is applied to pins 6 and 7 of the MC10124 translator (See Figure II-1). Pin 6 is the common strobe (enable) input for the translator and pin 7 is the signal input. Thus the AFIT IC gate signal acts to enable the translator

as well as to provide the input signal. The ECL 10K output appears at pin 3 and provides the necessary ECL 10K input to the Plessey SP8735B High Speed Divider at pin 16. This accomplishes the gating function for the T-Chain portion of the AFIT IC.

There are no connections between the MC10124 translator and the SP8735B High Speed Divider of the DCSO clock loop because the C-Chain of the AFIT IC is free-running and does not need to be gated. The interconnections between the Plessy SP8735B and the Motorola MC10124 are shown in Figure II-1.

AFIT IC (Ref. 16:2-17). In order to miniaturize the control electronics for the DCSO, an integrated circuit (hereafter referred to as the AFIT IC) was designed by four AFIT students in 1982. Maj G. R. Sims, Capt B. R. Varnum, Capt N. D. Hall, and 1Lt P. G. Staubs used Gate Universal Arrays (GUAs) to implement Boolean logic functions required of the DCSO controller circuit. They used the RCA TCS-093 GUA for the AFIT IC. The RCA TCS-093 is a Complimentary Metal Oxide/Silicon on Sapphire (CMOS/SOS) chip which measures 0.240 inches square. It contains 632 cells, each containing two "p" and two "n" transistors. A more detailed description of this integrated circuit is contained in the interim report, "LSI Implementation of a Digitally Compensated SAW Oscillator Controller Circuit", published by the Air Force Institute of Technology.

The AFIT IC contains three major units as shown in Figure II-5. The first section is the counter chain (C-chain) which divides the clock frequency and derives a gating signal for the controller circuitry. The C-chain measures time intervals by counting cycles of the clock oscillator. It consists of a 24-stage ripple counter with multiplexers at the clocking inputs of the second through eleventh stages. The multiplexers select either the external C-oscillator signal or the output from the previous counter stage as the input to the following stage. Four C-stage select lines are decoded to determine which one of the multiplexers passes the C-oscillator signal. The rest of the multiplexers pass the previous stage's output. The only input to the first stage is the oscillator signal. All of the stages before the one with the oscillator input are effectively cut off from the counter chain. Thus, the C-chain select lines vary the number of counting stages from 13 to 24. This provides a measure of flexibility in both the frequency of the oscillator used and the degree of precision in the overall compensation system.

The most significant bit of the counter is used as a gate signal for the thermometer chain (T-chain). When it goes high, it indicates the end of the counting period for the T-chain. At that time, the T-oscillator signal is gated off at the prescaler and the T-chain stops counting. The C-chain continues counting in order to provide timing for the control logic.

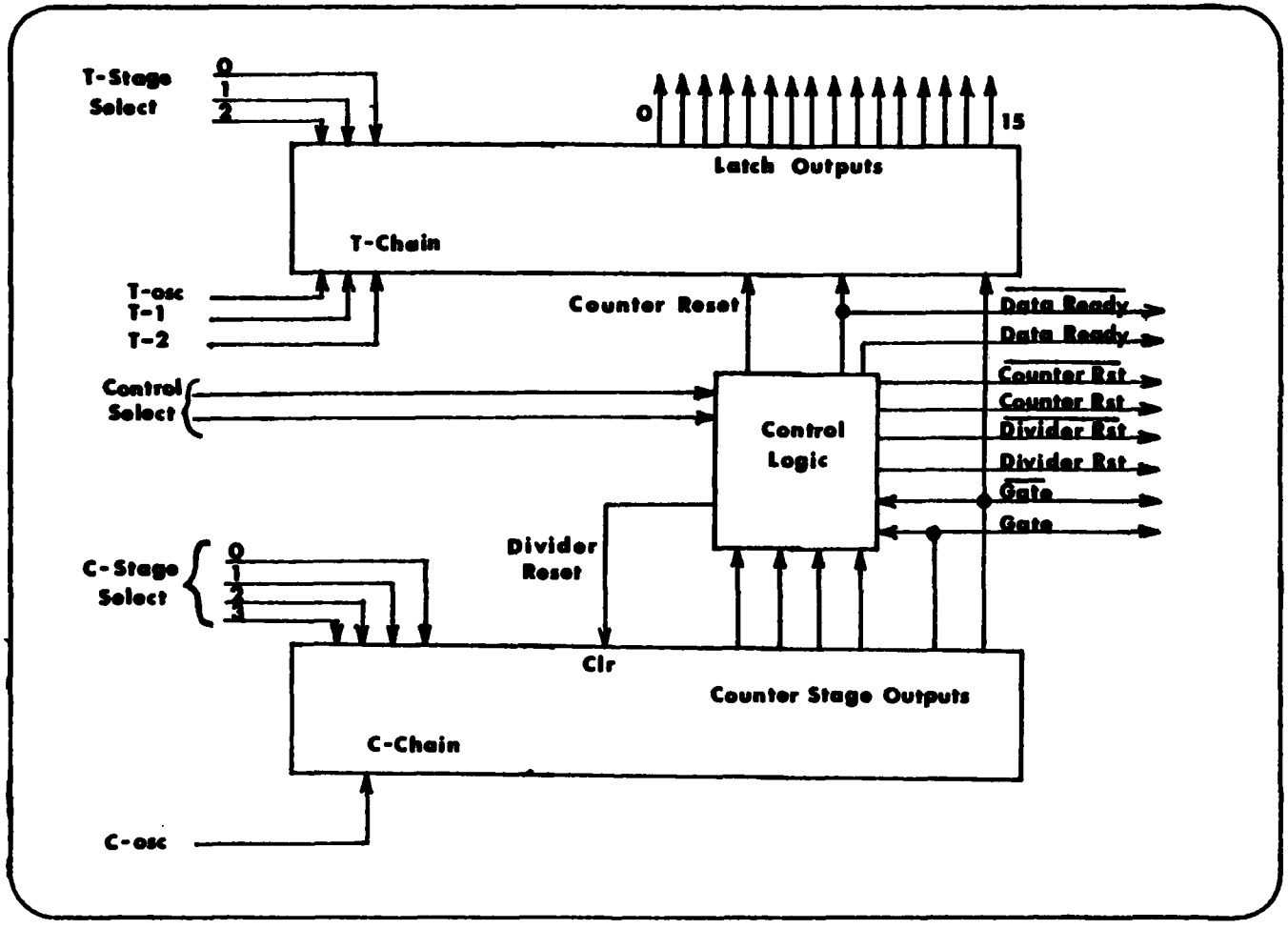


Fig. II-5 - AFIT IC Block Diagram
(Ref. 16:2-17)

The T-chain is similar to the C-chain, but it has 20 counting stages, and multiplexers on the inputs to the second through seventh stages. There are three T-stage select lines which cause the T-oscillator signal to be input to any one of the first seven stages. The length of the T-chain can thus be varied from 13 to 20 stages, effectively. In addition, the sixteen most significant bits of this counter have data latches which hold the count accumulated during the gated time interval. In order to make all sixteen of the data outputs valid when less than sixteen stages of the counter are being used, there are three multiplexers, located at the inputs to the three least significant data latches. These multiplexers select the appropriate inputs from the prescaler for the T-chain oscillator so there are always sixteen valid data bits in the latched outputs.

The control logic section produces three signals in sequence that strobe the T-chain stage outputs into the latches, clear the T-chain, and clear the C-chain in that order. They are called Data Ready, Counter Reset, and Divider Reset, respectively.

The connections for the AFIT IC are shown in Figure II-1. The jumper connections are provided so the length of both the C-chain and T-chain can be varied by simply tying the desired T-chain and/or C-chain select lines either high or low thus providing the proper binary code on the select lines.

Intel 2716 EPROM. The connections for the 2716 EPROM's are shown in Figure II-1. Two EPROM's are required in order to get 16 bit wide words. However, only 12 bits of the control word can be used since the D/A converter is limited to 12 input bits. The 2716 accommodates only 11 address bits from the AFIT IC. Since this is the case, only bits A0 through A10 of the AFIT IC are used.

There are 28 pin sockets provided for the second 2716 EPROM. This allows three additional signals ($\overline{\text{Divider Reset}}$, $\overline{\text{Counter Reset}}$, and $\overline{\text{Data Ready}}$) to be made easily available for the calibration process. The remaining unused pin can be used as a termination point for jumpers to other signals which may be needed for calibration and/or test points.

There is no biasing circuitry required for the EPROM's. The only requirement is for +5 volts and ground.

Feedback Circuitry.

The feedback circuitry can be thought of as the Burr-Brown D/A converter, the Op Amp circuit, and the phase shifter circuit. Each of these is discussed in the sections that follow.

Burr-Brown DAC85CQ-CBI-V D/A Converter. Although the DAC85 is only a 12 bit D/A converter, it should be adequate for this project. The DAC85 is wired to deliver 0 to +10 volts out using a complimentary straight binary (CSB) input. This is accomplished by connecting pin 15 to pin 19, pin 17

to pin 21, and pin 16 to pin 24. The CSB input means that if all 12 input bits are low, the D/A converter output is the full scale value of +10 volts. Conversly, if all 12 input bits are high, the D/A converter output is 0 volts. The D/A output is somewhere between these two values for any other combination of the 12 input bits.

No special biasing network is required for the DAC85, however, for best high frequency performance and noise rejection, power supply decoupling capacitors are connected as shown in Figure II-1. The 1.0 micro-farad capacitors should be located close to the DAC85 and should be tantalum or electrolytic types bypassed with a 0.01 micro-farad ceramic capacitor (Ref. 4:5-78).

Op Amp Circuit Design (Ref. 13:445-457). Since the signal to be amplified is a voltage signal, a voltage-sample voltage-sum (VSVS) configuration was chosen. As the term implies, the output voltage signal of the amplifier is sampled and the result is summed at the input. A common VSVS amplifier circuit is shown in Figure II-6.

Voltage sampling generally reduces the value of the output resistance (R_o) and makes the gain of the amplifier relatively independent of the load resistance (R_L). The input resistance (R_i) to the overall amplifier stage is given by:

$$R_i = \frac{R_B R_{in}}{R_B + R_{in}} \approx R_B \qquad \text{Eq. II-5}$$

since the input resistance (R_{in}) of the amplifier is theoretically infinite. Also, the output resistance of the amplifier (R_o) is approximately zero.

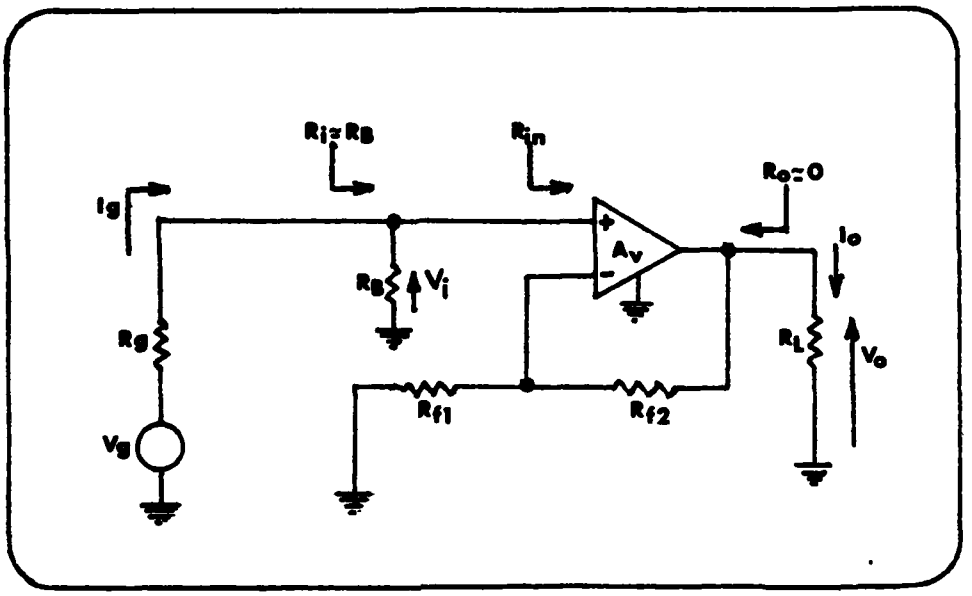


Fig. II-6 - Voltage-Sample Voltage-Sum Amplifier. (Ref. 13:454).

The generator-to-input voltage gain (A_{vg}) is given by:

$$A_{vg} = \frac{V_i}{V_g} = \frac{R_i}{R_i + R_g} \qquad \text{Eq. II-6}$$

where R_g is the generator resistance. For best performance, the circuit should be designed so that A_{vg} is approximately unity.

The negative feedback voltage gain is given by:

$$A_{fv} = \frac{V_o}{V_i} \approx \frac{R_{f1} + R_{f2}}{R_{f1}} \qquad \text{Eq. II-7}$$

and the generator-to-output (or overall) voltage gain of the amplifier stage is:

$$A_{vo} = \frac{V_o}{V_g} = A_{vg} A_{vo} \qquad \text{Eq. II-8}$$

The resistances chosen for R_B, R_{f1}, and R_{f2} cannot be chosen indescriminantly, but there is a wide range of flexibility available in deciding how large or small they should be. The biasing resistor (R_B) should be chosen so that the generator-to-input voltage gain remains near unity. The amplifier designed for this project uses a 100K ohm resistor for R_B but it could just as well have been something less.

The amplifier design for this project is shown in Figure II-7. The circuit uses variable resistors (trim pots) in the feedback loop to allow for a limited degree of gain adjustment. Using a 30K ohm resistance for R_{f2} and a 15K ohm resistance for R_{f1} gives an overall amplifier gain (A_{vo}) of 3, which is necessary to get a 0 to +30 volt output swing for the input to the phase shifter circuit.

Both a trim pot and a fixed resistor (100 ohms) are used in the amplifier input line. This is a requirement made necessary by the LM3900N op amp. Since the LM3900N operates on a single +32 volt supply, it makes use of a current mirror to achieve the non-inverting input function. Because of this, a limiting resistor is needed in series with the input lead when the amplifier is driven by a low-impedence source (Ref. 9:194). The output impedence of the D/A converter is approximately 0.05 ohms (Ref. 4:76) and the trim pot allows enough adjustment so the amplifier will

not saturate too soon as the D/A output transitions from 0 to +10 volts. The 100 ohm fixed resistor is used as a safety measure in that shorting of the LM3900N input could cause it to draw excessive current and fail.

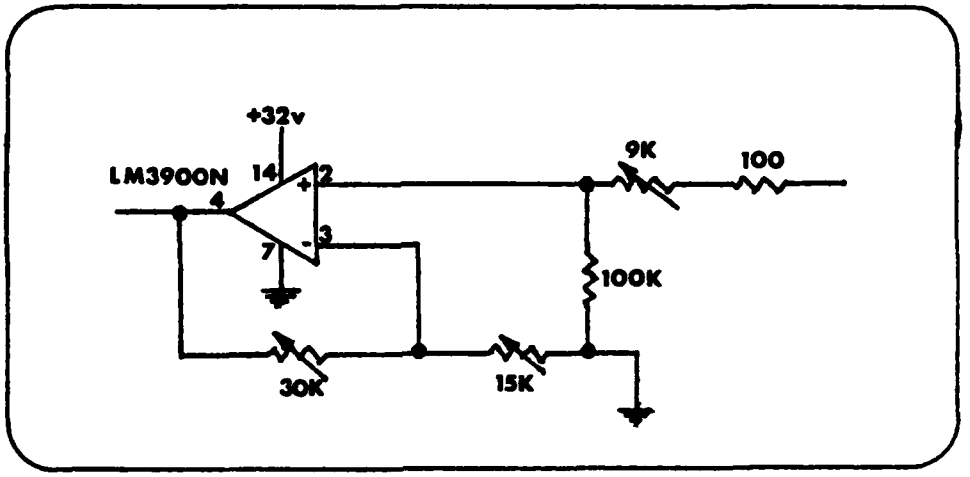


Fig. II-7 - Amplifier for DCSO Circuit Board.

Therefore, in the event the trim pot is adjusted to its maximum travel such that it becomes a short, the 100 ohm resistor will still protect the LM3900N from destruction.

Phase Shifter Design (Ref. 20:479-487). A reflector type phase shifter circuit using varactor diodes and a 3 dB quadrature hybrid coupler was chosen for this project. This type of circuit is almost always the best choice for a phase shifter since transmission type circuits are limited as to how much phase shift can be obtained and still maintain a good VSWR. The circuit diagram is shown in Figure II-8.

The first consideration was the size of the capacitors and inductors to be used. The capacitive reactance (X_C)

should be much less than the transmission line impedance of 50 ohms. Choosing X_C to be 1.0 ohm, the value of the capacitors is:

$$c = \frac{1}{2\pi f X_C} = \frac{1}{2\pi(300MHZ)(1.0\ ohm)} = 530\ pf \qquad \text{Eq. II-9}$$

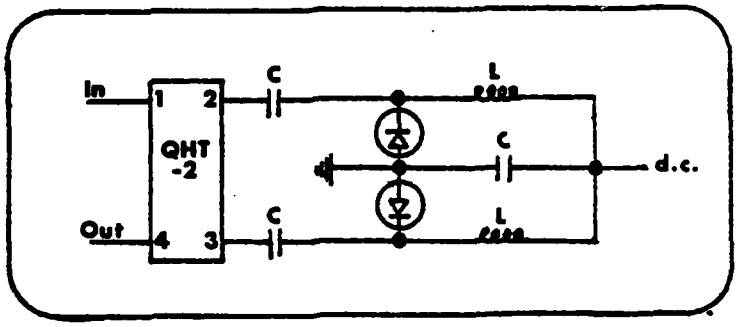


Fig. II-8 - Phase Shifter Circuit (Ref. 10:55).

Since 1000 pf UHF capacitors were readily available, they were used instead of 530 pf. Letting C equal 1000 pf, rearranging Eq. II-9, and solving for X_C gives a new value for capacitive reactance of 0.53 ohms.

For the RF chokes, the inductive reactance (X_L) should be much greater than the transmission line impedance. Choosing X_L to be 500 ohms, the value of the inductors is:

$$L = \frac{X_L}{2\pi f} = \frac{500\ ohms}{2\pi(300MHZ)} = 265nhy \qquad \text{Eq. II-10}$$

470 nhy inductors were used instead since they were already on hand. This does not degrade the performance of

the phase shifter since rearranging Eq. II-10 and solving for X_L gives an inductive reactance of 886 ohms which is much greater than the transmission line impedance of 50 ohms.

The next considerations are how much phase shift can be obtained as well as how much loss can be expected for the phase shifter circuit. It is necessary to look ahead at the end result for the phase shift magnitude which is given by:

$$|\Delta\phi| = 2 \tan^{-1} \frac{\frac{\Delta X}{Z_o}}{1 - \left(\frac{\Delta X/Z_o}{2}\right)^2} \qquad \text{Eq. II-11}$$

where

$$\Delta X = \frac{1}{2\pi f} \left(\frac{1}{C_{min}} - \frac{1}{C_{max}}\right) \qquad \text{Eq. II-12}$$

From Eq. II-11, it can be seen that the phase shift magnitude will be 180 degrees if $\Delta X/Z_o$ is equal to 2.0. This requires ΔX to be 100. This is approximately the amount of phase shift that will be needed for proper compensation of the DCSO clock frequency. Knowing this, the analysis can then proceed by determining the values of maximum capacitance (C_{max}) and minimum capacitance (C_{min}) for the MSI HA1717 varactor diode.

Since the diode has a 7:1 capacitance ratio, and C_{max} is 22 pf (Ref. 11:12), the minimum capacitance is 3.1 pf. However, for 180 degrees of phase shift, C_{min} must be (from

Eq. II-12) 4.27 pf. This presents no problem because the value of C_{min} can be directly controlled by slightly limiting the input voltage swing to the phase shifter circuit from the LM3900N op amp.

Using C_{max} = 22 pf, C_{min} = 4.27 pf, f = 300 MHz, and Z_o = 50 ohms, the phase shift magnitude (from Eqs. II-9 and II-10) can be verified as 180 degrees.

The insertion loss of the phase shift circuit is:

$$\text{Insertion Loss} = \frac{P_{incident}}{P_{reflected}} = 20 \log_{10} \frac{1+R/Z_o}{1-R/Z_o} \qquad \text{Eq. II-13}$$

where R is the diode resistance.

To calculate R, the cutoff frequency of the diode must be determined. Given that the Q factor of the HA1717 varactor diode is 850 at 50 MHz (Ref. 11:12) and assuming a linear relationship, the Q factor at 300 MHz should be 142. Then the cutoff frequency of the diode is:

$$f_c = Qf = (142)(300\ MHZ) = 42.6\ GHZ \qquad \text{Eq. II-14}$$

Now, the diode resistance is:

$$R = \frac{1}{2\pi C_{min} f_c} = \frac{1}{2\pi(4.27pf)(42.6GHZ)} = 0.87 \text{ ohms} \qquad \text{Eq. II-15}$$

Using R = 0.87 ohms and Z_o = 50 ohms, the insertion loss is (from Eq. II-14) 0.30 dB.

The figure of merit (F) for the continuous phase

shifter is defined as the number of degrees of phase shift per dB of loss and is given as:

$$F = \frac{\Delta\phi \text{ (deg)}}{\text{Loss (dB)}} = \frac{(115 \text{ deg})(\Delta X/Z_o)}{0.30 \text{ dB}} = 766.7 \frac{\text{deg}}{\text{dB}} \qquad \text{Eq. II-16}$$

The loss over the calculated range of the phase shifter is then:

$$\text{Loss} = \frac{1 \text{ dB}}{766.7 \text{ deg}} (180 \text{ deg}) = 0.235 \text{ dB} \qquad \text{Eq. II-17}$$

Taking into account the 3 dB loss of the quadrature hybrid coupler, the total loss of the phase shifter is 3.235 dB. This is well within the 5 dB loss that was originally allowed in designing the DCSO clock loop.

Total Power Consumption.

The total power consumption of the DCSO circuit board was predicted by considering the power typically drawn by the active components. In some cases, the component specifications listed the input current and voltage requirements. Then the power was calculated from Power = (Input Current)(Voltage). In other instances, the typical power was listed in the specifications. The power dissipated by the AFIT IC was calculated by using the average of the input current readings observed during testing.

The active components and their respective power

requirements are listed in Table II-1. It can be seen that the total power for the DCSO circuit is nearly six watts. The two MICamps account for about 35.5% of the total power while the two Intel 2716 EPROMs account for about 17.8% of the total power.

Table II-1.

DCSO Circuit Power Consumption.

Component	Qty.	Current	Voltage	Power
MICamp	2	+70 mA	+15 v	2.100 W
LM3900N	1	---	+32 v	.570 W
D/A Conv.	1	+25 mA	+15 v	.375 W
		-25 mA	-15 v	.375 W
		+20 mA	+ 5 v	.100 W
SP8735B	2	-80 mA	-5.2v	.832 W
MC10124	1	-72 mA	-5.2v	.374 W
		+25 mA	+ 5 v	.125 W
2716	2	---	+ 5 v	1.050 W
AFIT IC	2	+16 mA	+ 5 v	.008 W
			Total =	5.909 W

Circuit Board Design

Initially, a rough sketch (not to scale) of the circuit board layout was done. This was used as a starting point in determining the best use of the IC pin configurations and the best placing of the individual components. After the rough sketch was finished, a layout drawing (to scale) was completed.

A 4:1 artmaster tape-up of the board layout using red and blue tape on a sheet of clear mylar film was the next step. The mylar, normally .005 to .007-in. thick, is temperature stable and provides a smooth non-porous surface

to which the tape and patterns adhere (Ref. 8:121).

Taping Standards (Ref. 8:126-127). Regardless of taping methods or type of material, the physical act of taping must conform to some basic standards.

Conductor angles should be made at preferred angles of 30, 45, or 90 degrees. Although the traces could be directed at almost any angle, it is important that all traces running parallel be at the same angle for uniformity. The minimum angle that any trace should be placed at is 90 degrees. Angles less than 90 degrees provide a situation which could allow etching solution to build up on the inside angle and etch away too much material.

Traces should not come any closer to the edge of the board than .050-in. at a scale of 1 x 1 inch and, if at all possible, at least .100-in. should be left. This allows the necessary tolerance that is required to shear the board to the size specified. If less distance is left, a portion or all of a trace could get sheared off or shorted out.

There should be no overlapping of tape or cutting of pads. Tape has a natural tendency to "creep" or return to its original shape if it is bent or stretched at all. Even under the most careful conditions, this can be a problem so care must be taken not to create even more difficult situations where tape could distort and cause electrical and manufacturing problems.

Taping Method. The red and blue tape method was used because it made alignment of the front and back sides of the board easier. Black pads were used when a pattern was desired on both the front and back sides of the board. The red tape was used to lay out the front side of the board and the blue tape was used to lay out the back side of the board. This method allowed the photographer, by use of red and blue filters on his camera, to filter out the blue tape in one case and photograph only the red tape. By changing filters, the photographer was able to photograph the blue tape and filter out the red tape. The advantage to this method was that the tape-up did not have to be flipped over during the process and absolute registration for the two sided PC board was obtained.

Red and blue tape is not easy to work with because of its rigid polyvinyl composition. It is more difficult to cut and takes more care to ensure that it will stick to the base mylar. Red and blue tape cannot be bent without distortion of the traces; therefore, it has to be cut all the way through and repositioned each time the direction of the run is changed (Ref. 8:125).

DCSO Board Tapeup. For the DCSO circuit board, taping standards were adhered to as much as possible. The digital portion of the board presented no special taping problems. Standard 4:1 IC pads were used and .062-in. tape was used for the traces. When reduced to original size, this gave

traces that were .0155-in. (15.5 mils) wide.

More care had to be taken in taping out the RF portion of the DCSO circuit board. The width of the 50 ohm transmission lines had to be .174-in. $\pm$ .002-in. (174 $\pm$ 2 mils). This was the manufacturer's specification for the 3M CuClad 250 GX teflon/glass laminate used to manufacture the board. In order to obtain this width, a strip of .500-in. (500 mils) tape was laid beside (and butting against) a strip of .200-in (200 mils) tape. A third piece of .200-in. tape was then laid over the butting edges to ensure that a uniform metal pattern would result. This gave a trace .700-in. wide which, when reduced to original size, gave a width of .175-in. (175 mils).

Constant radius bends were also needed which meant that much cutting was required whenever the direction of the trace was changed. A template and razor blade was used for this purpose.

The ground plane was obtained by covering the entire reverse side of the RF portion of the board with tape, being careful to overlap it to ensure a continuous metal surface would result. Again, using a template and razor blade, non-functional terminal areas were obtained by cutting away portions of the tape. Where component leads terminated at the ground plane, the same procedure was used except that a piece of .200-in. tape was placed across the bare area for an electrical connection. This ensured that the ground plane would not act as a "heat sink" during soldering of the

leads thus causing inferior or "cold" solder joints. The DCSO circuit board is shown in Figures II-9 and II-10. Overall dimensions of the final board were 7.28 inches by 3.72 inches.

Package Design.

A package was designed to enclose the DCSO circuit board. The final dimensions were 4.00-inches wide, 7.55-inches long, and 1.22-inches deep. The package was fabricated from aluminum and plexiglass by personel at the AFIT Model Shop. A photograph of this package is shown in Figure II-11 and the design diagrams are given in Appendix E.

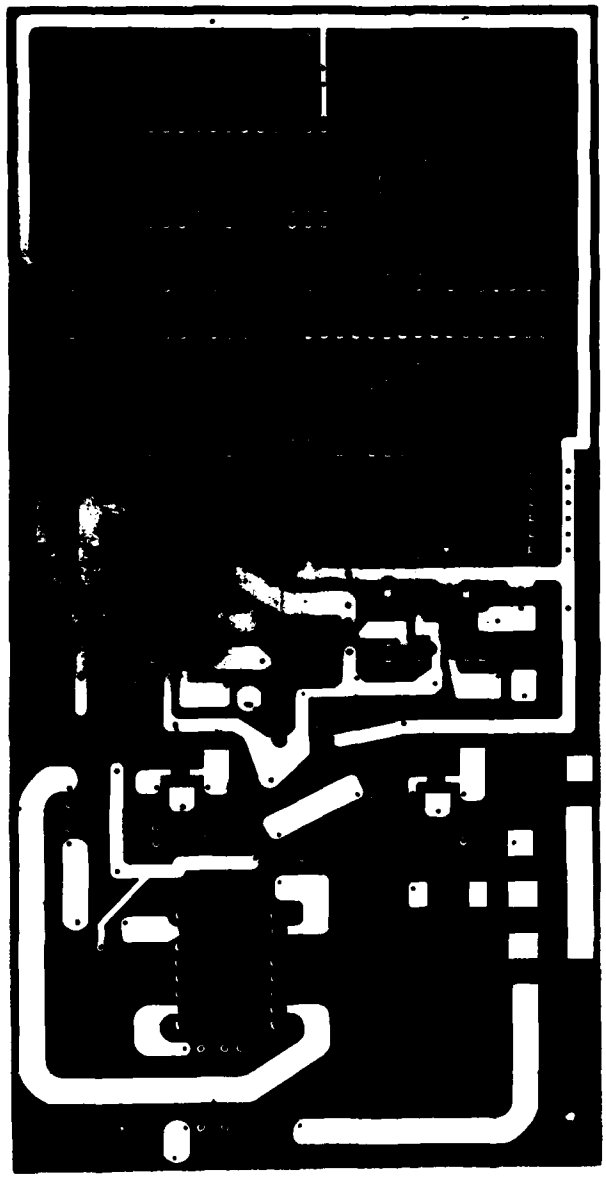


Fig. II-9 - DCSO Circuit Board (Front Side)

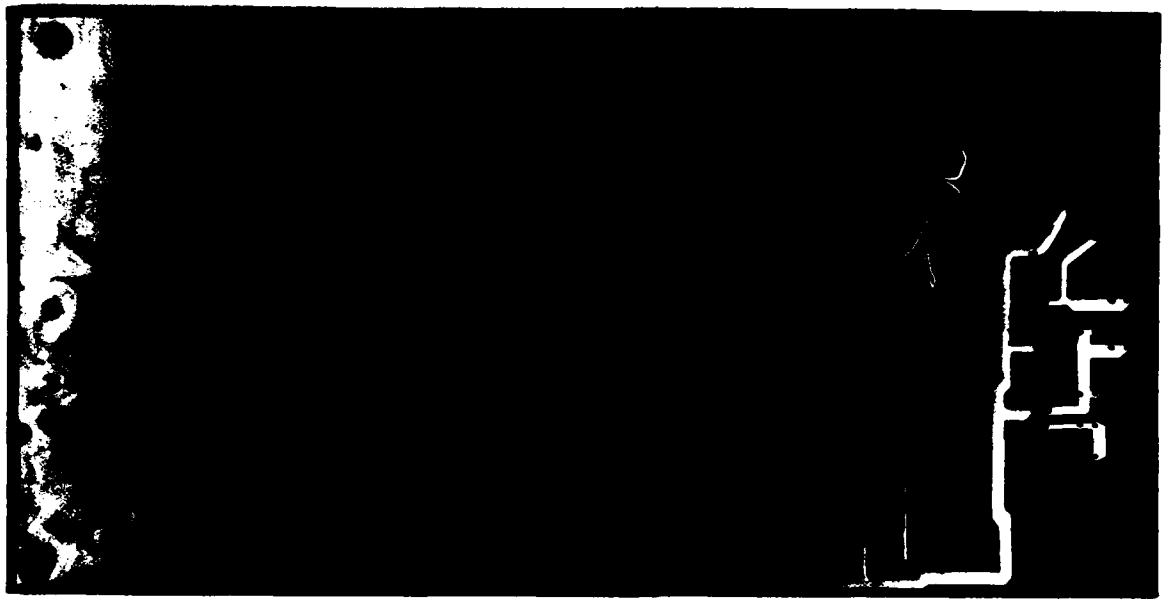


Fig. II-10 - DCSO Circuit Board (Back Side)

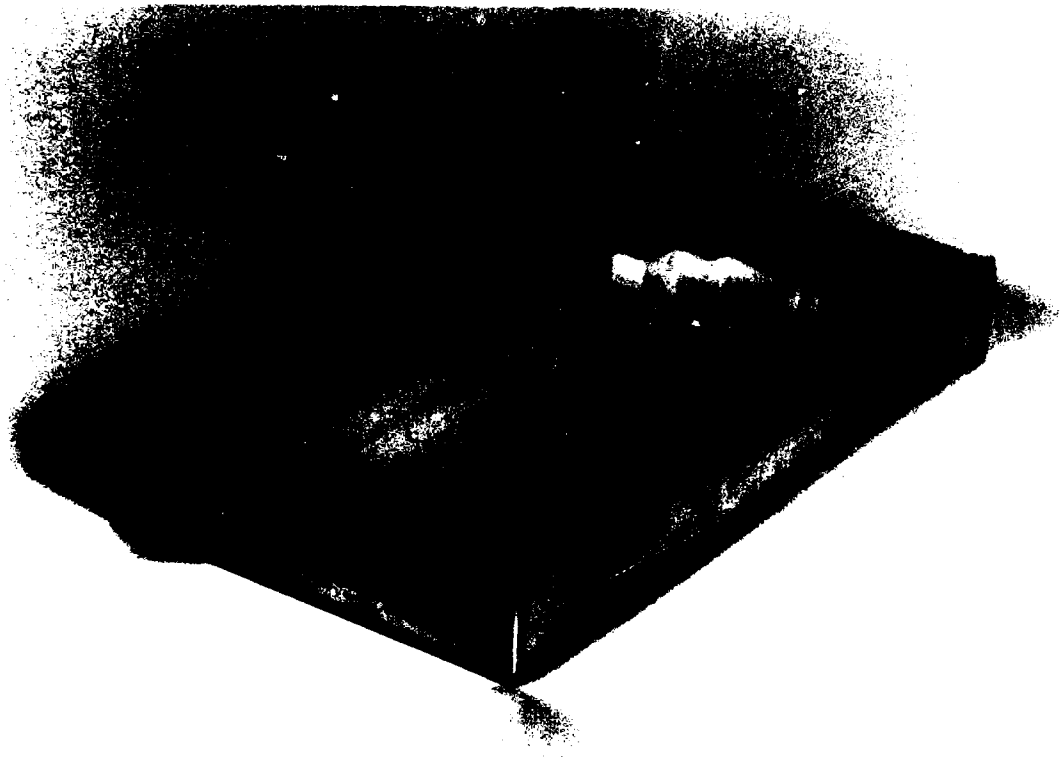


Fig II-11.- DCSO Package

III. Test Procedures and Results

Testing of the DCSO circuit was performed by breaking the circuit into individual sections. This procedure allowed greater flexibility in simulating the input parameters to a particular section of the circuit and insured that the output parameters of the section under test could be interpreted accurately since miscellaneous inputs from other parts of the circuit were eliminated. In some instances, only one component was considered as a section. For example, the AFIT IC, a complex CMOS/SOS chip, needed to be tested at the gate level. Therefore, the AFIT IC could not be tested in conjunction with other components until it was shown to function properly.

Some circuit sections were constructed by wiring them up on a "proto board" while others required fabrication of special test circuit boards. The "proto board" approach to testing was used for some of the digital circuitry. Special circuit boards were fabricated in order to test portions of the RF circuit where 50 ohm transmission lines were needed.

RF Circuitry.

Testing the RF circuitry included verifying proper operation of the UTO MICamps and DS-109 power divider. Also, the SAW device was tested to determine the insertion loss, impedance, and VSWR. The PCA attenuators were assumed

to function properly.

UTO-524 MICamp/ DS-109 Power Divider. Four Avantek UTO-524 MICamps were ordered for this project . In order to insure that these devices would be ready when needed, they were tested to verify that they met the advertised specifications.

First, each amplifier was numbered so it could be identified later. Then, each amplifier was soldered into place on a prototype circuit board that was later used in tuning the RF feedback loops. The DS-109 power divider was also included in the transmission path. D.C. power was applied to the MICamps and a Hewlett Packard 608D signal generator was used to provide an input signal for the MICamp. An ammeter was connected in series with the d.c. supply so that the input current to the MICamp could be recorded. A Cutler-Hammer 707 spectrum analyzer was used to observe the MICamp output. Table III-1 summarizes the results.

Table III-1

Measured MICamp Parameters.

MICamp	Input Current	Input Signal	Input Freq.	Gain	Saturated Output
1	83.4 mA	-30 dBm	300 MHz	36 dB	+20 dBm
2	69.0 mA	-30 dBm	300 MHz	36 dB	+17 dBm
3	69.2 mA	-30 dBm	300 MHz	32 dB	+17 dBm
4	65.1 mA	-30 dBm	300 MHz	33 dB	+17 dBm

All four MICamps operated above minimum specifications, however, it was noted they all oscillated on their own. This was thought to be caused by the coaxial cable (used in the test set-up) acting as a tuning stub and providing positive feedback in the loop. The performance of the DS-109 power divider was also satisfactory.

SAW Tests. The SAW device was tested for three parameters: 1) Insertion loss, 2) Impedance, and 3) VSWR. To test for these parameters, a special circuit board was fabricated and used in an existing test fixture. This test fixture, shown in Figure III-1, allowed free access to each of the four SAW ports.

Insertion Loss. A Hewlett Packard 608D signal generator and Cutler-Hammer 707 spectrum analyzer were used to determine the insertion loss of each port of the SAW device. First, the spectrum analyzer was calibrated by connecting a coaxial cable directly from it to the signal generator. The resultant amplitude response of the spectrum analyzer was noted and used as a baseline. Next, the SAW path under test was connected between the coaxial cables, and the signal generator was adjusted to the resonant frequency of the SAW path. The insertion loss of the clock path (port 1 to 2) was measured as 18.5 dB at a resonant frequency of 298 MHz. The insertion loss of the thermometer path (port 3 to 4) was measured as 16 dB at a resonant

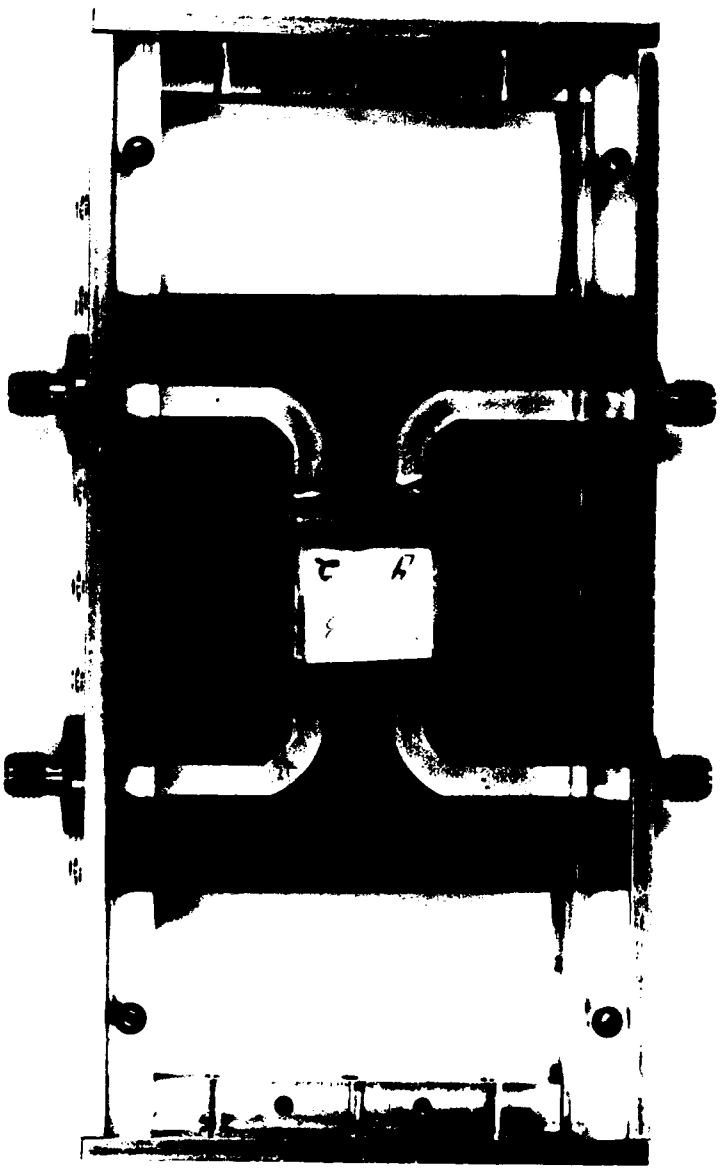
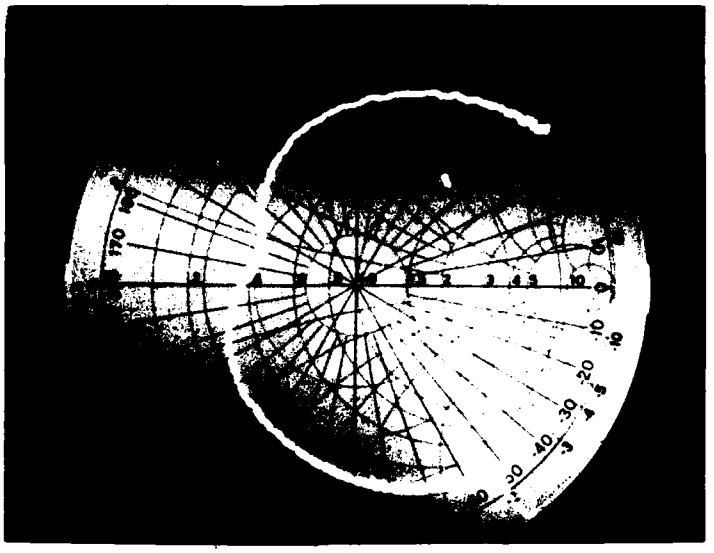
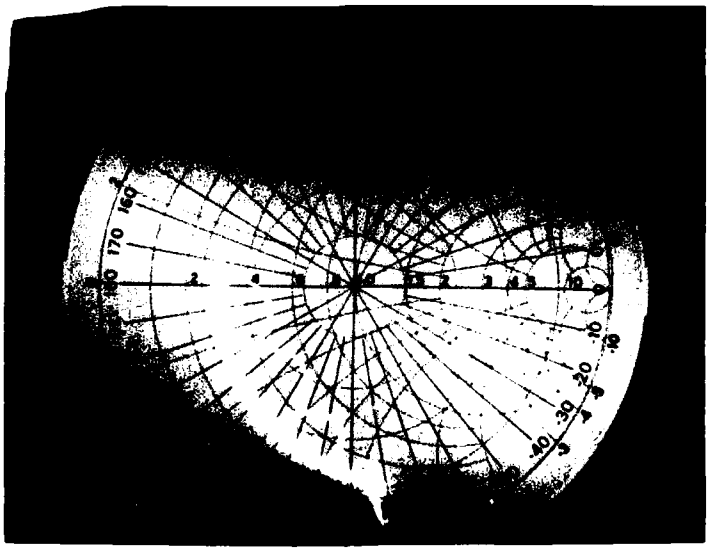


Fig. III-1 - SAW Test Fixture

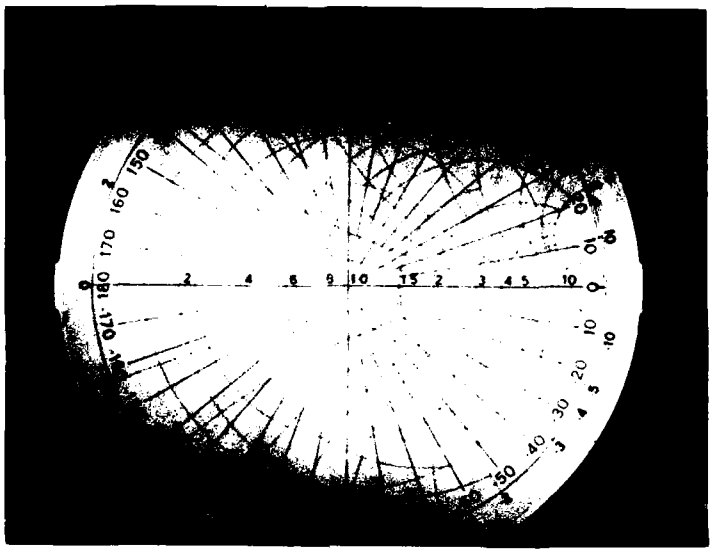


(a) Port 1

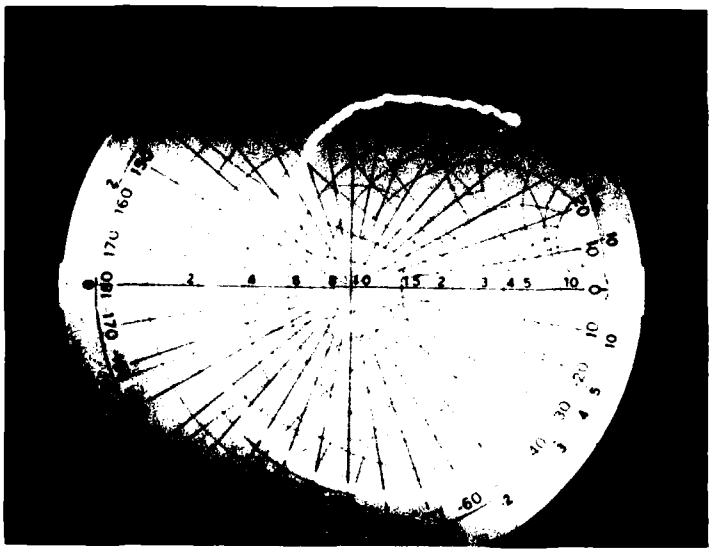


(b) Port 2

Fig. III-2 - SAW Impedance Polar Plots



(c) Port 3



(d) Port 4

Fig. III-2 – SAW Impedance Polar Plots

frequency of 309 MHz.

Impedance and VSWR. A Hewlett Packard 8690B sweep oscillator and a Hewlett Packard 8410A network analyzer with a polar display were used for measuring the impedance and VSWR of each SAW port. First, the polar display was calibrated using a 50 ohm load and then a short. The sweep oscillator was set to sweep the frequency range from 248 MHz to 335 MHz, and each port of the SAW device was connected, one at a time, to the test port on the reflection test unit. The VSWR and normalized impedance of the SAW port under test were read directly from the Smith Chart overlay on the polar display. Photographs of the polar display for each SAW port are shown in Figure III-2a through d. The measured VSWR and normalized impedance, as well as the resonant frequencies of each SAW port, are given in Table III-2.

Table III-2

SAW Test Results.

Port	Normalized Impedance	Resonant Frequencies	VSWR
1	0.4+j.15	298 MHZ	2.5
2	0.4-j1.0	251 MHz	5.0
	0.5-j0.7	274 MHz	3.0
	0.55-j0.4	298 MHZ	2.2
	0.48-j0.1	320 MHz	2.1
3	0.68-j0.6	261 MHz	2.2
	0.8-j0.2	284 MHZ	1.4
	0.9+j0.1	309 MHz	1.2
4	0.4+j0.4	309 MHz	2.9

The actual impedance is obtained by multiplying the normalized impedance by the characteristic impedance of the transmission line (Zo=50 ohms). The VSWR was obtained by observing where the circle of constant radius (from the center of the Smith Chart to the normalized impedance point) crossed the right hand side of the real axis.

Digital Control Circuitry.

The only part of the digital control circuitry tested was the AFIT IC. The Plessy SP8735B, Motorola MC10124, and Intel 2716 EPROMs were not tested.

AFIT IC. Testing of the AFIT IC was performed in several steps. First, a visual inspection of the individual chips was performed. Selected chips were then bonded to a 48 pin dual-in-line package (DIP). Each chip was then tested for proper operation of the various divider and selector stages which make up the T-chain, C-chain, and control logic. The input current to the AFIT IC under test was also noted. All chips were visually inspected and twelve chips were selected for testing.

Visual Inspection. Approximately eighty chips were received from NCR. These chips had already been diced and placed in sectional compartments in a plastic carrier. The carrier (with chips enclosed) was placed under a microscope

was visually inspected. Overall, the chips having sharp, clear patterns, and clean ver, there were some problems.

run around the edge of a couple of chips had em. An example of this defect is shown in In general, the edges of all the chips were a few cases, the ground run was broken. An defect is shown in Figure III-4.

of what appeared to be a chemical film were eral chips and washing one of the chips in to remove the substance. Since the chips had with a coating of glass, the substance was cted from the acetone. An example of this in Figure III-5.

mmon defect was black blotches that appeared the surface of several chips. Again, these not be rinsed away with acetone. An example is shown in Figure III-6.

. A Kulicke & Soffa Model 484 ultrasonic to bond the chips to the 48 pin DIP package. sure that static electricity did not harm the package was placed in a piece of conductive and this material was grounded to the bonder lip. The ground pad on the chip was bonded any other pads.

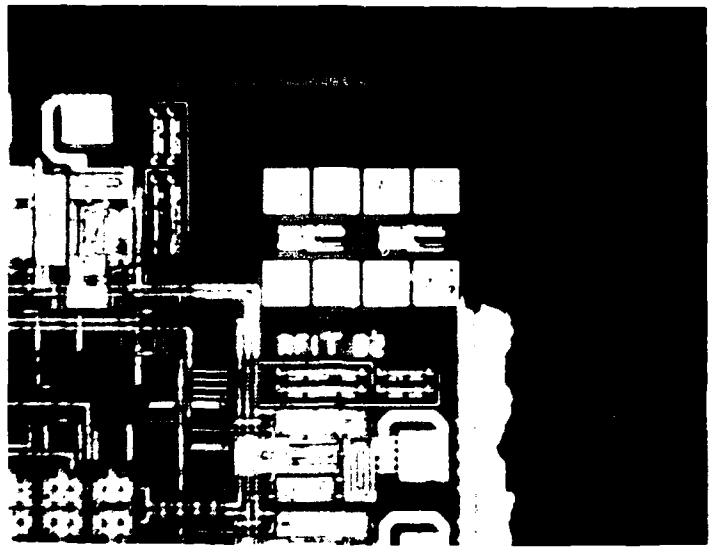


Fig. III-3 – AFIT IC Chip (Metal Missing)

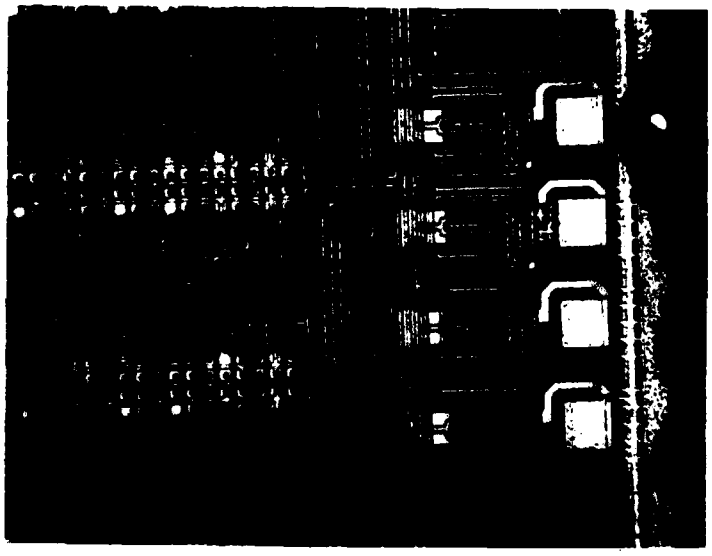


Fig. III-4 – AFIT IC Chip (Ground Run Broken)

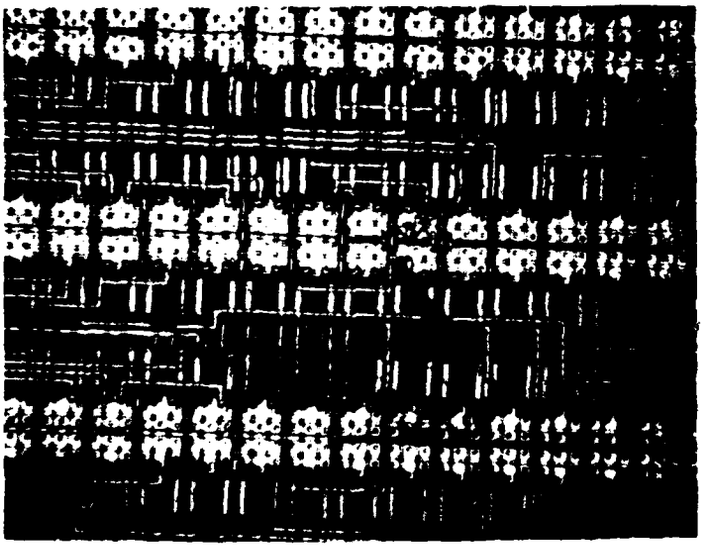


Fig. III-5 – AFIT IC Chip (Chemical Film on Surface)

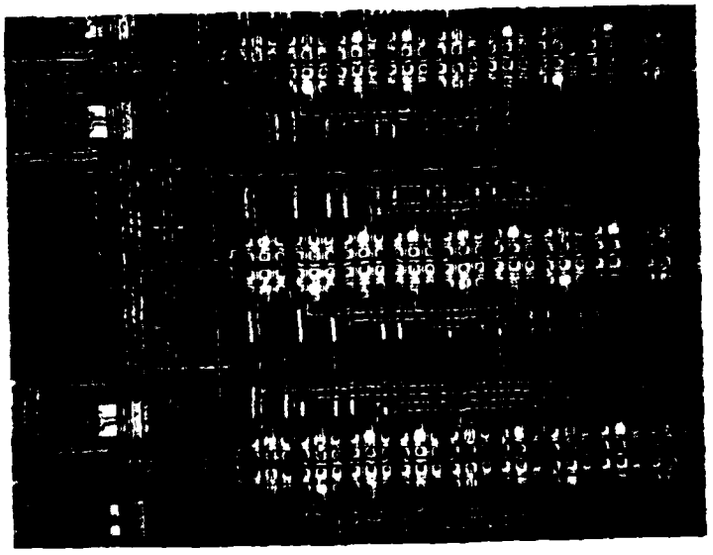


Fig. III-6 – AFIT IC Chip (Dirt on Surface)

Power Test. The power test was performed in order to determine the input current drawn by the AFIT IC. An ammeter was connected in series with the 5 volt supply to the chip (RD5) and power was applied. The input current was different for each of the twelve chips tested. The highest current measured was 25.9 mA while the lowest was 8.5 mA. Most current readings fell between 8.5 mA and 9.5 mA.

T-Chain Test. A schematic diagram of the AFIT IC is shown in Figures III-7a, b, and c, and the logic diagrams which make up the individual stages are shown in Figures III-8a through f. The intent of the T-chain test was to demonstrate that the IM Stage Selectors, TF Stages, OM Multiplexer, OM Stage Select, and DF Latches worked properly. Also, the Counter Reset and Data Ready functions needed to be verified.

In testing the IM300 Stage Select, a 5 volt, 100 Hz square wave was applied to the T-Osc input (BL4) and an oscilloscope was connected to the IM300 test point (LD6). Counter Reset (TR3) and Data Ready (TL3) were tied low. An exact replica (as expected) of the T-Osc input signal was observed at the IM300 test point. This is shown in Figure III-9.

The input frequency was increased to 600 KHz before the IM300 Stage Select output signal fell below 2 volts. By decreasing the amplitude of the T-Osc input signal to 3 volts, the maximum frequency of the IM300 Stage Select

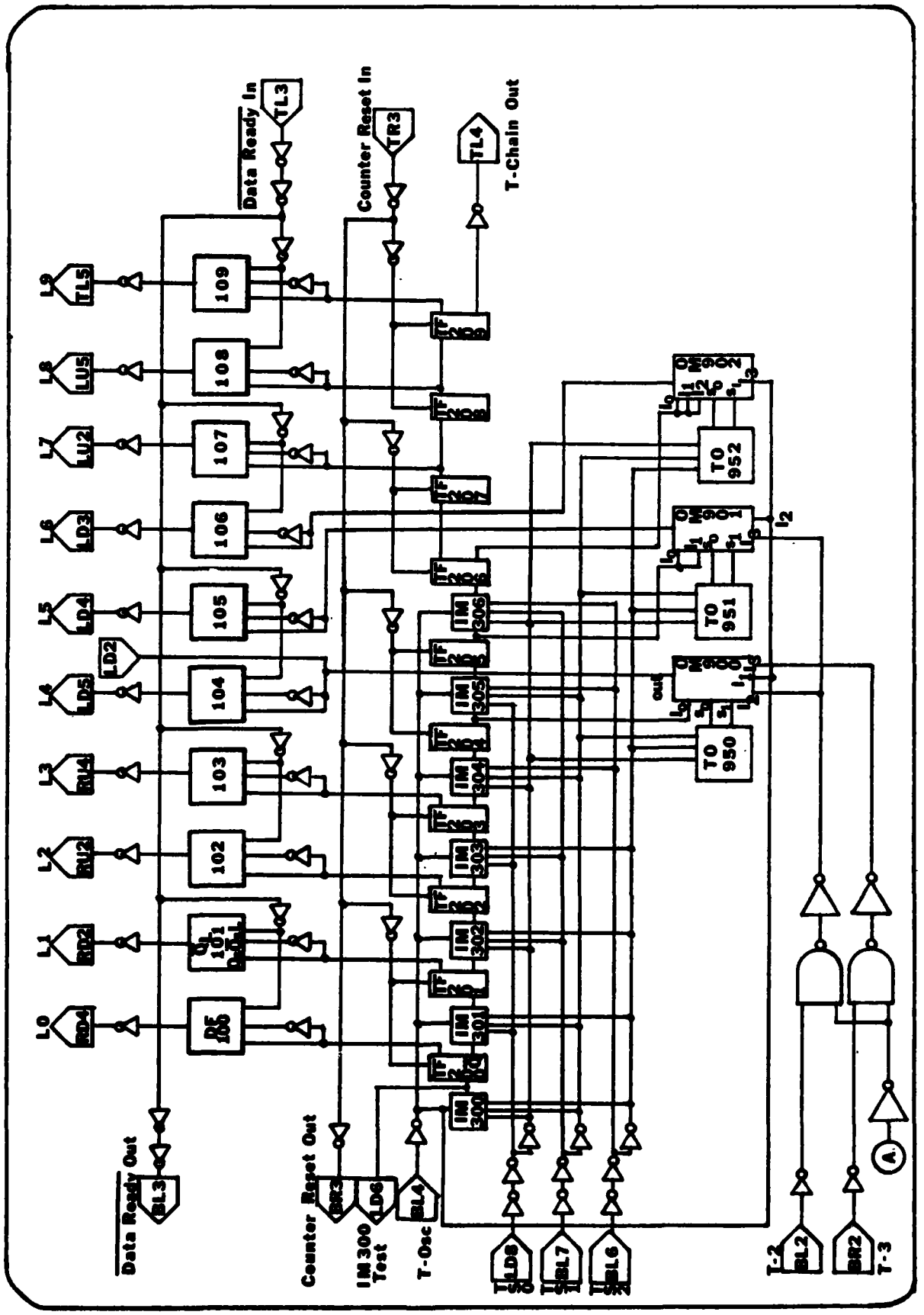


Fig. III-7a - AFIT IC T-Chain

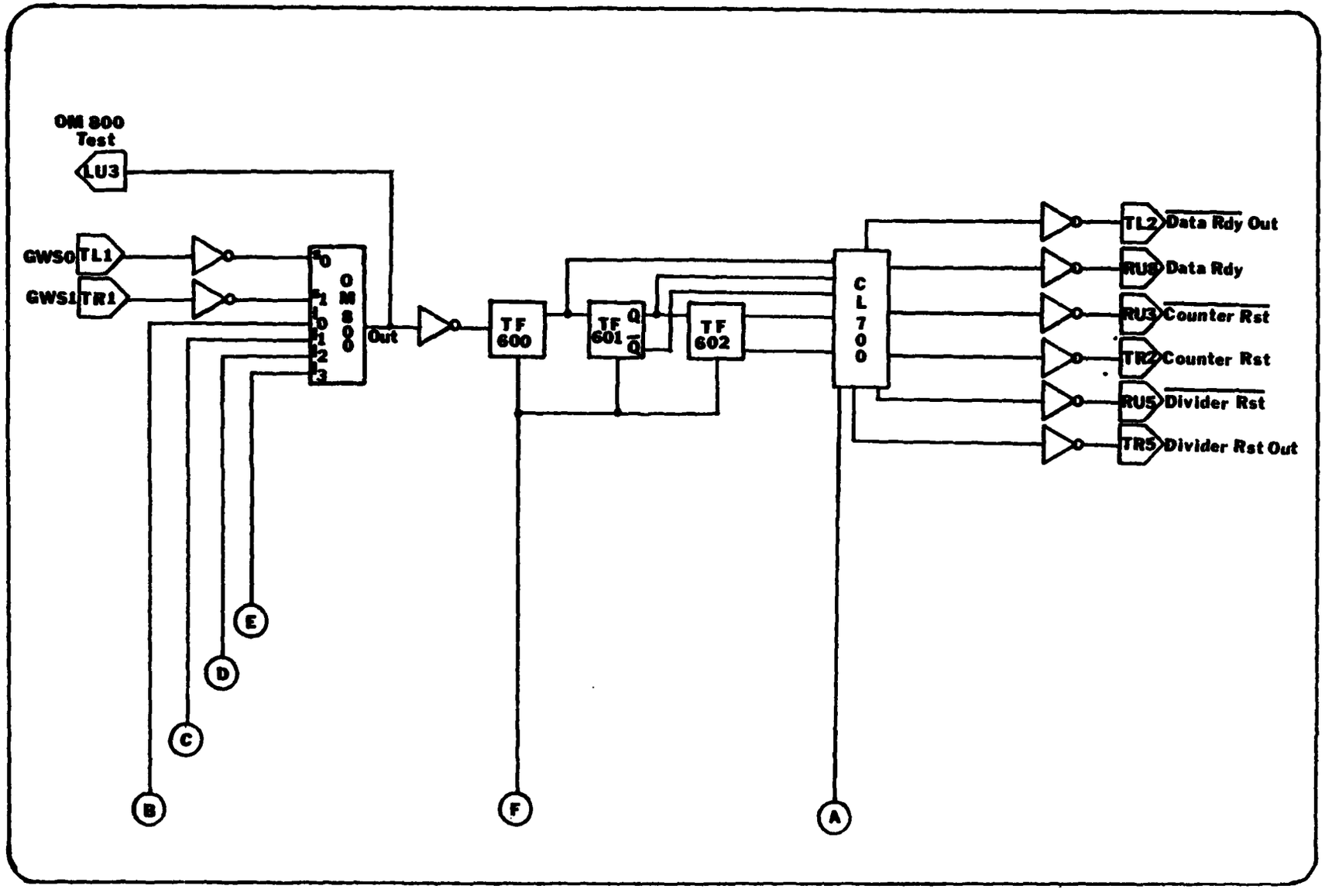


Fig. III-7b - AFIT IC Control Logic

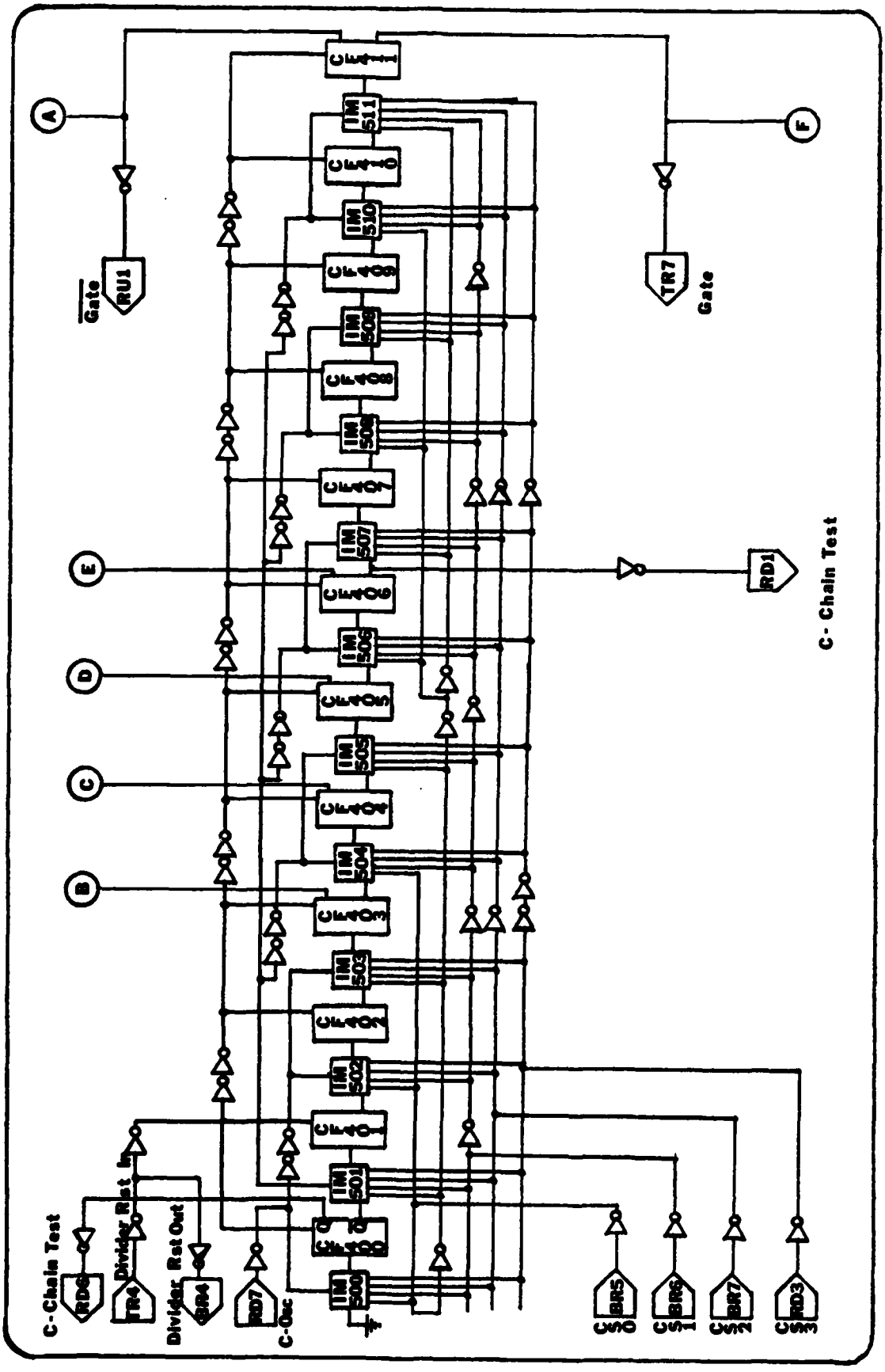


Fig. III-7c - AFIT IC C-Chain

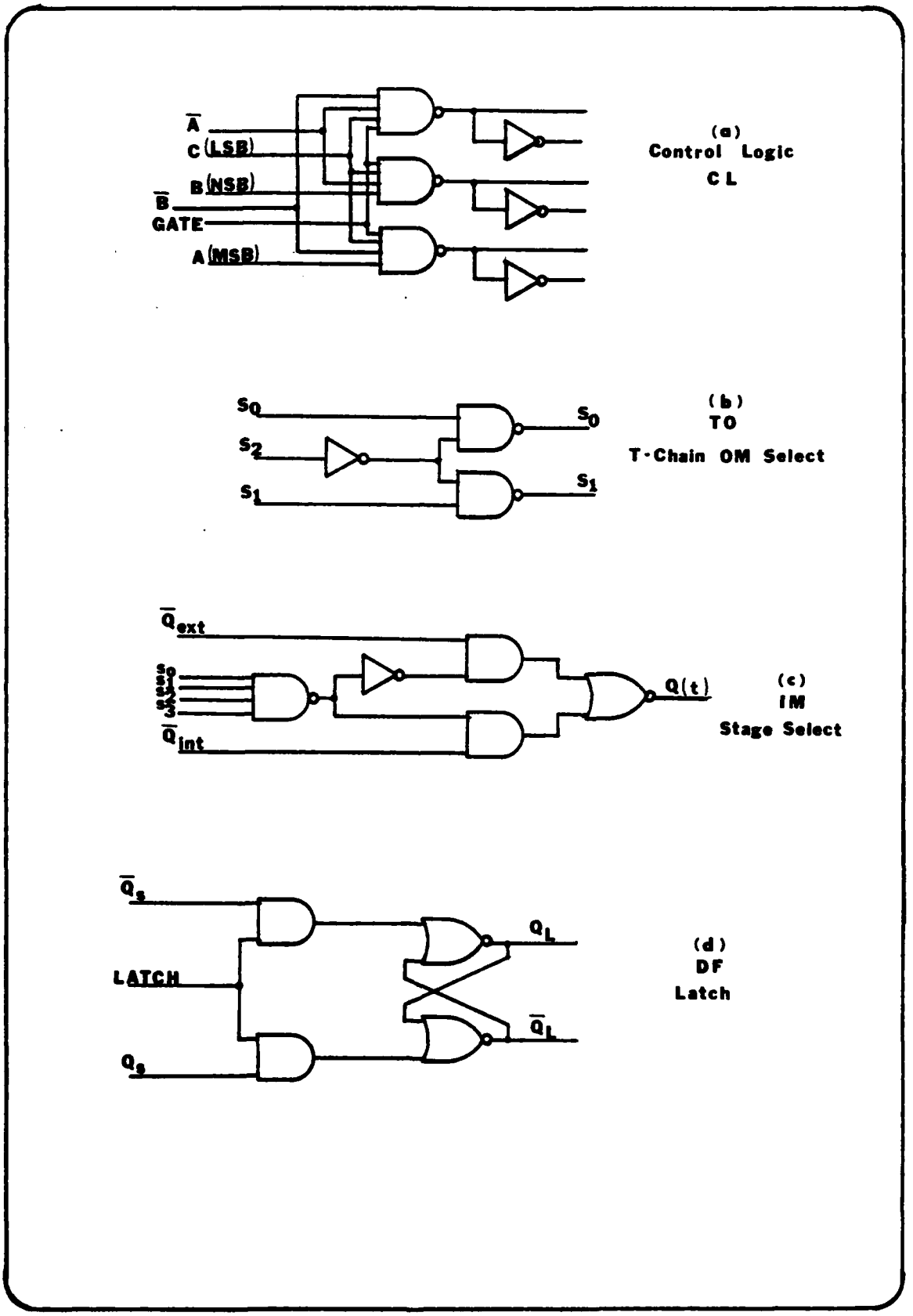


Fig. III-8 - AFIT IC Logic Diagrams

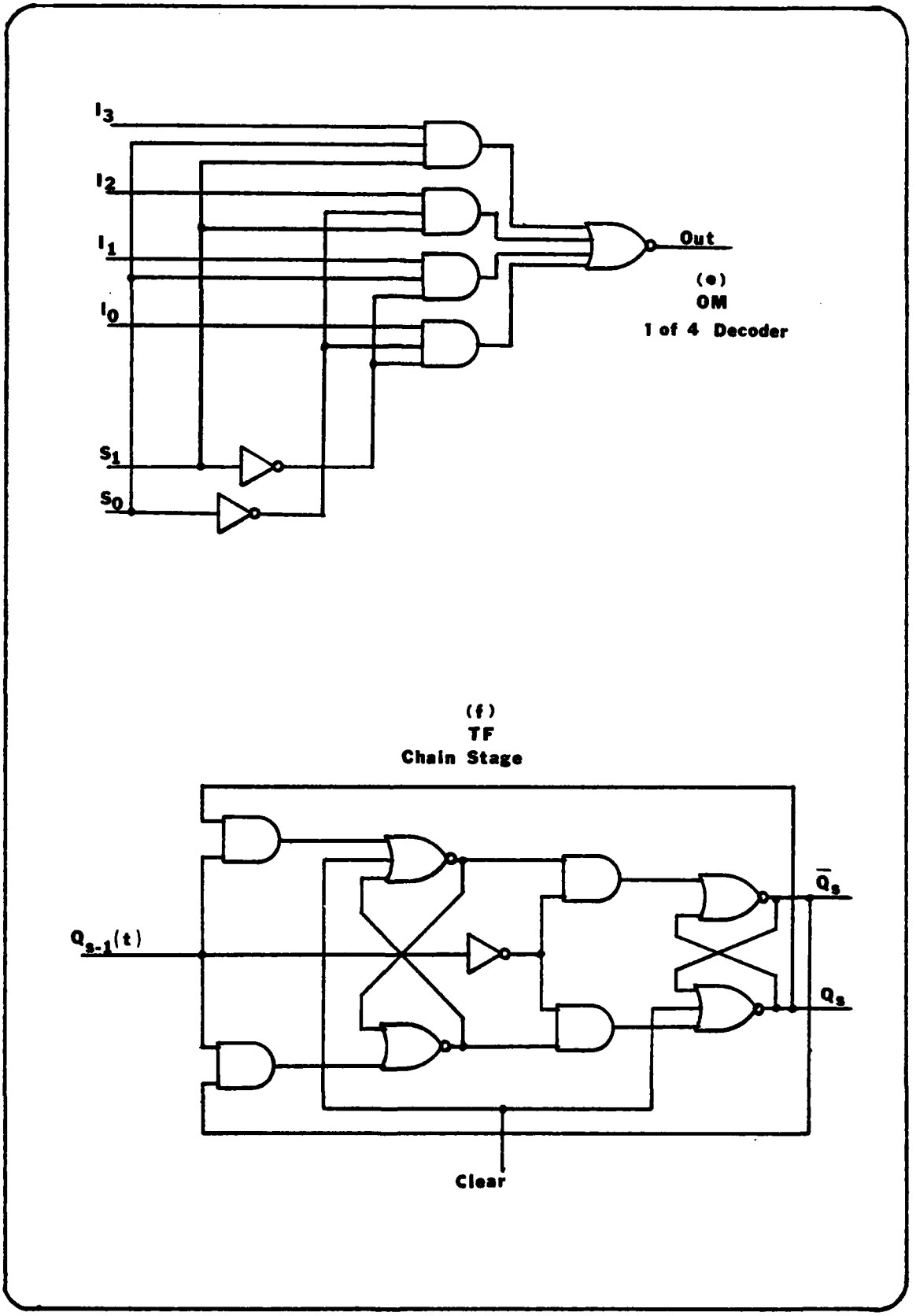


Fig. III-8 - AFIT IC Logic Diagrams

output signal rose to 1 MHz before again falling below 2 volts.

When any T-chain select line (TS0, TS1, or TS2) was tied high, the output signal of the IM300 Stage Select dissappeared as expected. This indicated that the IM300 Stage Select had been dropped from the T-chain.

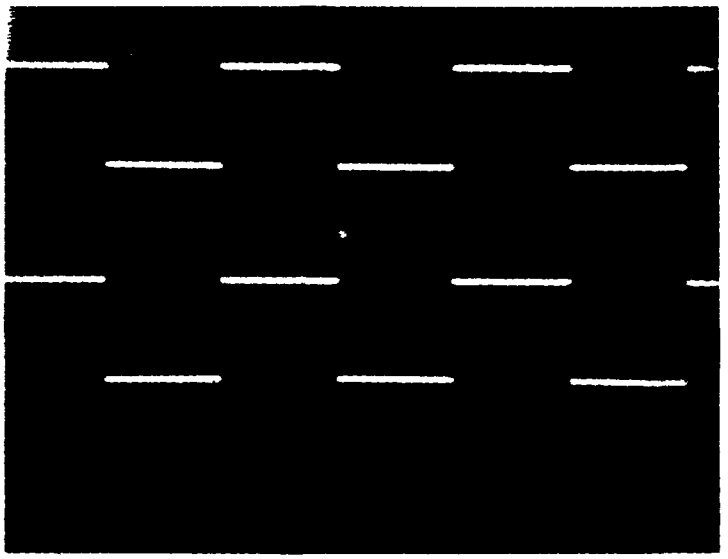


Fig. III-9 - IM300 Test Output.

In summary, the IM300 Stage Select operated properly on all twelve chips below 600KHz. Above 600KHz, the amplitude of the IM300 output signal fell below 2 volts.

The TF Stages and DF Latches were tested in conjunction with the T-chain select lines. (Programming the proper binary code on the select lines enables the proper IM Stage

Select. This, in turn, enables the corresponding TF Stage so the count displayed at the DF Latch outputs can be varied.) In effect, then, the IM Stage Selects were tested as well. Table III-3 indicates what should be observed at the DF Latch outputs given the select line inputs and a 5 volt square wave input at T-Osc (BL4).

Table III-3

DF Latch Outputs.

TS2	TS1	TS0	Stage	L0	L1	L2	L3	L4	L5	L6	L7	L8	L9
0	0	0	IM300	÷2	÷4	÷8	÷16	÷32	÷64	÷128	÷256	÷512	÷1096
1	1	0	IM301	N/A	2	4	8	16	32	64	128	256	512
1	0	1	IM302	N/A	N/A	2	4	8	16	32	64	128	256
1	0	0	IM303	N/A	N/A	N/A	2	4	8	16	32	64	128
0	1	1	IM304	N/A	N/A	N/A	N/A	2	4	8	16	32	64
0	1	0	IM305	N/A	N/A	N/A	N/A	N/A	2	4	8	16	32
0	0	1	IM306	N/A	N/A	N/A	N/A	N/A	N/A	2	4	8	16

On five of twelve chips, the TF200 Stage failed to work. This was evidenced by the absence of a divide-by-two signal at the L0 latch output (RD4) with TS2=0, TS1=0, and TS0=0. For the other select line codes, the latch outputs were as expected on all twelve chips; however, there was a noticeable lag between the time the input signal changed states and the output signal changed states. This lag time was subsequently measured as approximately 2 msec. An example of the latch output is shown in Figure III-10 where the top signal is the input to T-Osc and the bottom signal is the output of the L1 latch with a select line code of 000. The T-Osc frequency is 30 Hz. It can be seen from

Figure III-10 that the L1 latch output is asymmetric, having a slightly longer "off" time than "on" time. Also, the 2 msec lag time between the input and output signals is clearly evident and the input signal is not divided exactly by four. The maximum input frequency varied from chip to chip, but all were below 330 Hz. Further analysis of this phenomenon is given on page III-31.

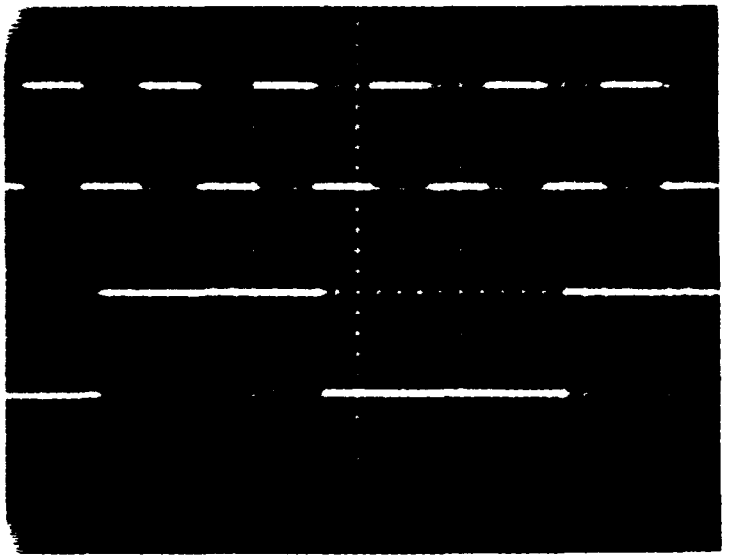


Fig. III-10 - T-Osc Input/L1 Output Showing Time Lag.

As a further test, light emitting diodes (LEDs) were connected to the latch outputs and a 10 Hz, 5 volt square wave signal was applied to the T-Osc input. The LEDs gave a visual indication that the TF stages were counting. When the Counter Reset line was tied high, all the latch outputs went high and remained high until the Counter Reset was again tied low.

In Summary, the TF stages could be selected properly. The TF stages, and DF latches did work, but not as expected. The TF stage output signals were asymmetric due to an approximate 2 msec switching time lag which limited the maximum input frequency to between 40 Hz and 330 Hz depending on which chip was tested. Further, the TF 200 stage was inoperative on five of twelve chips. Finally, the Counter Reset function worked properly.

The OM900 1 of 4 Multiplexer and OM Select (TO 950) were tested together. In order to save time, these functions were tested on only two chips. An attempt was made to select each of the four input signals (I0, I1, I2, and I3) to the OM900 multiplexer and observe the output at the OM900 test point (LD2). Table III-4 shows the binary code needed on the select lines in order to select the indicated input signal to the OM900 multiplexer.

Table III-4

Select Codes and Output Signal of OM900.

TS0	TS1	TS2	I0	I1	I2	I3
0	0	1	1	0	0	0
1	0	1	0	1	0	0
0	1	1	0	0	1	0
1	1	0	0	0	0	1
1	1	1	0	0	0	1
0	0	0	0	0	0	1

A 5 volt, 100 Hz square wave signal was applied to the T-Osc input (BL4). The T-2 and T-3 input pads were tied

high and no signal was applied to the C-Osc input which effectively eliminated a signal at point A in Figure III-7a. When a 001 was programmed on the T-chain select lines, a replica of the T-Osc input signal was observed at the OM900 multiplexer output. The output signal should have been I0, a "divide-by-two" version of the T-Osc input signal, because the 001 code selects IM304 which causes the T-Osc signal to be divided by two through the action of TF204. The output of TF204 is the I0 input of the OM900 multiplexer. Programming the select lines for all eight codes (000 thru 111) failed to produce a "divide-by-two" signal at the OM900 test point. Also, no other signals were observed except for the 001 code. These results indicated that the OM900 multiplexer input signal being selected was actually I1 which is connected directly to the T-Osc input. The I1 input signal could not be selected with the proper code (101). Malfunction of the TF204 stage was ruled out since it had already been shown to function properly on the same two chips under test.

Next, the OM900 multiplexer was tested to see if the I2 input could be selected. The T-Osc signal was removed and the T-Osc pad (BL4) was tied low. A 5 volt, 100 Hz square wave was applied to the T-2 input pad (BL2) and the T-3 input pad (BR2) was tied high. When a 011 was programmed on the select lines, the input signal at T-2 was <u>not</u> observed at the OM900 test point as expected. All eight codes (000 thru 111) were programmed on the select lines with the

result that only a 101 code produced a signal at the OM900 multiplexer output test point. The input signal was varied in frequency, and the corresponding change in frequency was observed in the output signal. These results indicated that although the I2 input was being selected, it was being selected by the wrong code.

Finally, the OM900 multiplexer was tested to see if the I3 input could be selected. Again, the T-Osc input was tied low and no input signal was applied to the C-Osc input pad. The T-2 input (BL2) was tied high and a 5 volt, 100 Hz square wave signal was applied to the T-3 input (BR2). Programming all eight codes on the select lines produced an OM900 multiplexer output signal only for 011, which is the I2 select code. Again, the input signal was varied in frequency with a corresponding change in the output signal. These results indicated that although I3 was being selected, it was being selected by the wrong code.

On both chips, the results were the same. Table III-5 lists the select codes and the resulting signal selected.

Table III-5

OM900 Test Results.

TS0	TS1	TS2	I0	I1	I2	I3
0	0	1	0	1	0	0
0	1	1	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	0
0	0	0	0	0	0	0

In all of the OM900 multiplexer and TO950 selector tests, the maximum frequency of the output signal was approximately 350 KHz. Above this frequency, the amplitude of the output signal fell below 3 volts as shown in Figure III-11 where the top signal is the input and the bottom signal is the output of OM900.

In summary, the I0 input could not be selected at all, and the other three inputs (I1, I2, and I3) were selected by the wrong codes as indicated in Table III-5.

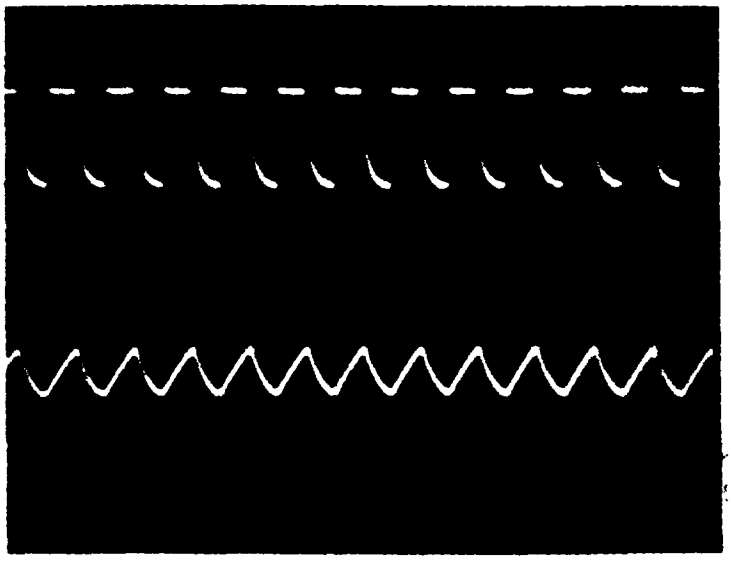


Fig. III-11 - OM900 Multiplexer Output Above 350 KHz.

C-Chain Tests. Testing of the C-chain was done in order to verify that the IM Select stages, and CF Divider stages worked properly. In addition to showing that the IM Select stages worked properly when selected, it was necessary to

demonstrate that the proper select code enabled the correct IM stage.

The C-chain is almost identical to the T-chain except it has four select lines instead of three. Also, the C-chain has no latches. Each succeeding CF stage divides the input signal from the previous stage by two. Programming the proper binary code on the C-chain select lines (CS0, CS1, CS2, and CS3) causes a specific IM stage to enable it's corresponding CF divider stage. Any preceeding IM stages to the one selected are dropped out of the C-chain.

Unlike the T-chain, which performed basically the same on all chips tested, the performance of the C-chain was not repeatable from one chip to another. Two test points (RD6 and RD1) were available to test the C-chain. With a 5 volt square wave signal as the input to C-Osc (RD7) and with Divider Reset In (TR4) tied low, the IM and CF stages were tested according to Table III-6.

Table III-6

C-Chain Select Codes and Test Point Outputs.

CS3	CS2	CS1	CS0	Stage	RD6	RD1
0	0	0	0	IM500	÷2	÷128
0	0	0	1	IM501	0	÷64
0	0	1	0	IM502	0	÷32
0	0	1	1	IM503	0	÷16
0	1	0	0	IM504	0	÷8
0	1	0	1	IM505	0	÷4
0	1	1	0	IM506	0	÷2
0	1	1	1	IM507	0	0

For the first code (0000), a "divide-by-two" signal, as expected, was observed at RD6 on one chip. However, the signal was asymmetric, displaying a longer "off" time than "on" time. On many chips, there was either no output signal at RD6, or the output signal displayed even worse asymmetry than the T-chain had displayed. On still other chips, the output signal at RD6 was broken up, displaying no symmetry whatsoever. Two examples of the output signal at RD6 are shown in Figure III-12a and b. Of the twelve chips tested, only one chip displayed a "somewhat" correct output. No further testing was done on chips displaying an erratic output at RD6.

Using the chip which had displayed the most nearly correct output signal at RD6, the rest of the codes were programmed on the select lines and test point RD1 was monitored with an oscilloscope. It was evident that the select line codes were selecting the proper IM stages; however, the CF stages were not dividing exactly by two. For example, this can be seen from Figure III-13 where the select lines were programmed with 0011 and the output at RD1 was monitored. The top signal in Figure III-13 is the input signal to C-Osc and the bottom signal is the observed signal at RD1. The signal at RD1 should have been a "divide-by-16" but it was approximately a "divide-by-23" signal instead. This was due to the asymmetric property of the RD1 output signal.

The C-chain operated at a maximum of 600 Hz. Above

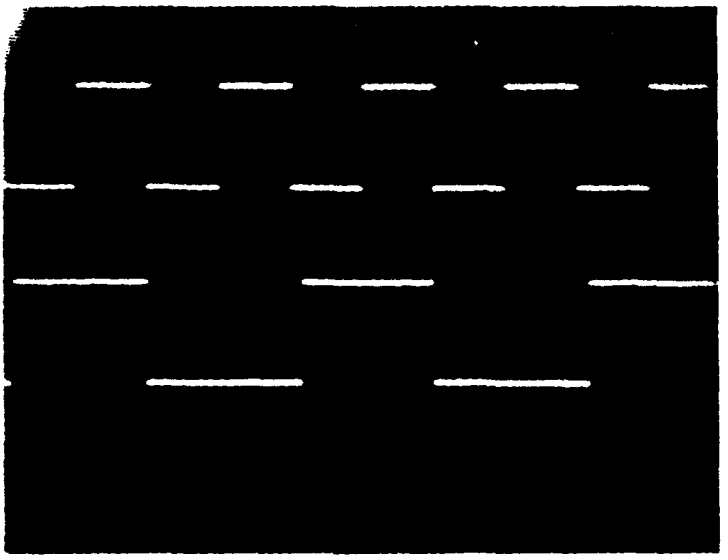


Fig. III-12a. RD6 Output (Divide-by-Two)
Frequency 200 hz

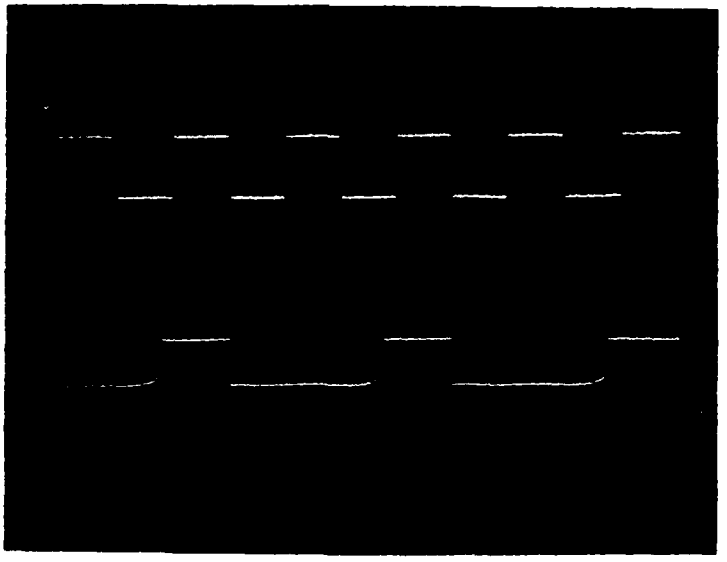


Fig. III-12b. RD6 Output (Asymetric)
Frequency 500 hz

this frequency, the output signals at both RD6 and RD1 became erratic and switched to a constant low output.

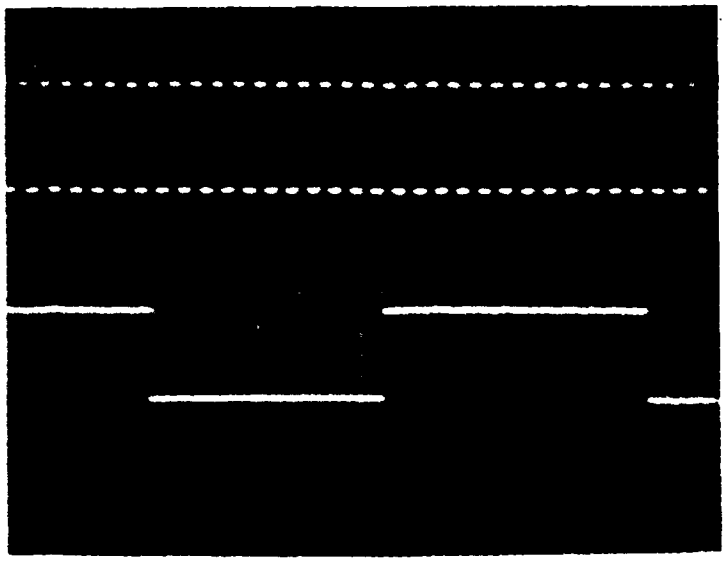


Fig. III-13 - RD1 "Divide-by-Sixteen" Output.

Control Logic. The control logic section was tested in order to verify proper operation of the OM800 multiplexer, the three TF stages (600, 601, 602), and the CL700 stage. Since an output signal from the C-Chain was needed in order to test the control logic, only the chip which displayed the "somewhat" correct C-Chain output signal was tested.

In order to test the OM800 multiplexer, a 5 volt square wave signal was applied to the C-Osc input (RD7). Then, IM503 through IM506 were enabled individually by programming the required code on the C-chain select lines. An

oscilloscope was connected to the OM800 test output (LU3). As each IM stage was enabled, the code which would allow the output signal from the correspondingly selected CF stage to pass through OM800 was programmed on the two OM800 select lines (GWS0, GWS1). For example, programming a 0011 on CS3, CS2, CS1, and CS0 enables IM503. IM503 selects CF403 which divides the C-Osc signal by two. The output of CF403 is the I0 input of OM800, and this signal should be seen at the OM800 output test point (LU3). Table III-7 gives the input conditions necessary to obtain the corresponding output conditions at the OM800 multiplexer test point.

Table III-7

OM800 Multiplexer Test Conditions.

Case	CS3	CS2	CS1	CS0	IM	CF	GWS1	GWS0	OM800 Select	OM800 Output
1	0	0	1	1	503	403	0	0	I0	÷2
2	0	0	1	1	503	403	0	1	I1	÷4
3	0	0	1	1	503	403	1	0	I2	÷8
4	0	0	1	1	503	403	1	1	I3	÷16
5	0	1	0	0	504	404	0	0	I0	0
6	0	1	0	0	504	404	0	1	I1	÷2
7	0	1	0	0	504	404	1	0	I2	÷4
8	0	1	0	0	504	404	1	1	I3	÷8
9	0	1	0	1	505	405	0	0	I0	0
10	0	1	0	1	505	405	0	1	I1	0
11	0	1	0	1	505	405	1	0	I2	÷2
12	0	1	0	1	505	405	1	1	I3	÷4
13	0	1	1	0	506	406	0	0	I0	0
14	0	1	1	0	506	406	0	1	I1	0
15	0	1	1	0	506	406	1	0	I2	0
16	0	1	1	0	506	406	1	1	I3	÷2

During this phase of testing, the C-chain stopped working. The C-chain output signal became erratic and indistinct so it was impossible to know if the signal was a divide-by-2, 4, 8, or 16. Therefore, all combinations listed in Table III-7 above could not be observed. However, by checking for cases 1, 6, 11, and 16, an erratic signal was also observed at the OM800 multiplexer test point. This sufficiently verified proper operation of the OM800 multiplexer. An example of the OM800 multiplexer output for case 1 is shown in Figure III-14. The top trace is the C-osc input signal, and the bottom trace is the broken, erractic OM800 output signal. The bottom signal should have been a divide-by-two version of the C-osc input. This erratic signal was due to the fact that the C-Chain was malfunctioning.

Because of the erratic output signal of the C-chain, the three TF stages could not be tested. The C-Osc signal was removed and the six outputs of the CL700 stage were recorded. Each signal was either high or low. The results are shown in Table III-8.

In addition to the twelve chips that were bonded and tested, approximately twelve unpackaged chips were tested with a probe. A signal was input to T-osc and the L0 output was monitored. This effectively tested the IM300, TF200, and DF100 stages. A divide-by-two signal, having a maximum frequency of about 300 Hz, was observed on six of these chips. All six chips exhibited the delay from master to

slave (TF 200) mentioned earlier, which resulted in an asymmetric output.

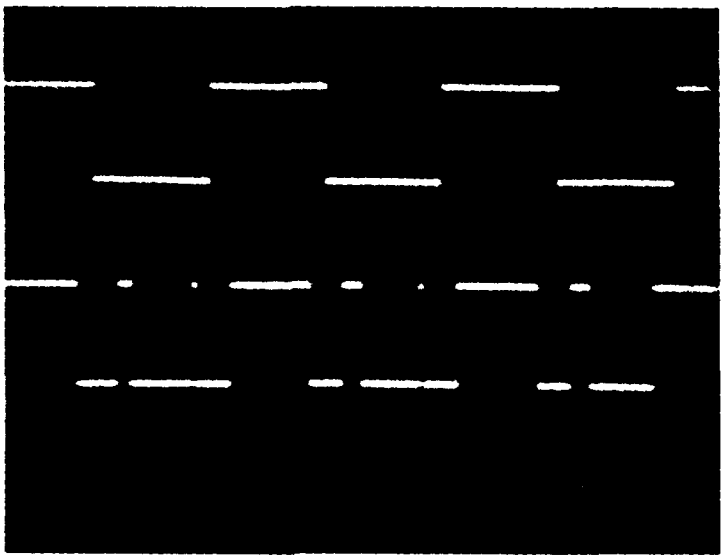


Fig. III-14 - OM800 Multiplexer Output (I0 Selected).

Table III-8

CL700 Output States.

Output Signal	State
$\overline{\text{Data Ready}}$	Low
Data Ready	High
$\overline{\text{Counter Reset}}$	Low
Counter Reset	High
$\overline{\text{Divider Reset}}$	Low
Divider Reset	High

A couple of things were done in investigating this problem. First, the TF flip-flop design was constructed using TTL gates, and verified to be logically correct. Next, the gate array design was re-examined. Finally, the

metal pattern (mask) was examined. It corresponded to the gate array design, and appeared to be defect free on the chip. Since some of the TF stages did not work at all, while others had various delays, it was concluded that either there were "opens" over some of the vias creating a large capacitance, or there was a high resistance at some of the vias, or some of the transistors and tunnels were defective.

Overall, operation of the AFIT IC was unsatisfactory for several reasons. On many chips, the TF200 stage did not function. Of the TF stages that worked, all exhibited a delay between the time of the input signal transition and the TF flip-flop transition. The maximum operating frequency of the T-Chain was 300 Hz. Operation of the C-Chain was even worse. Only one of twelve chips tested displayed a "somewhat" correct signal. This signal also displayed the switching time lag observed in the T-Chain signal. As a result of this time lag, the CF stage output signals were asymmetric, and the maximum operating frequency of the C-Chain was only 600 Hz. Finally, the T-chain OM select did not select the proper signals. Because of these flaws, it was determined that the AFIT IC chip could not be used in the circuit.

Feedback Circuitry.

The Feedback circuitry was tested in two steps. First, proper operation of the D/A converter and Op Amp circuit was

verified. Next, the phase shifter was tested in conjunction with the D/A converter and Op Amp circuit.

D/A Converter and Op Amp Circuit. The D/A converter and op amp were tested as a module by connecting them on a "proto board" in the configuration shown in Figure III-15.

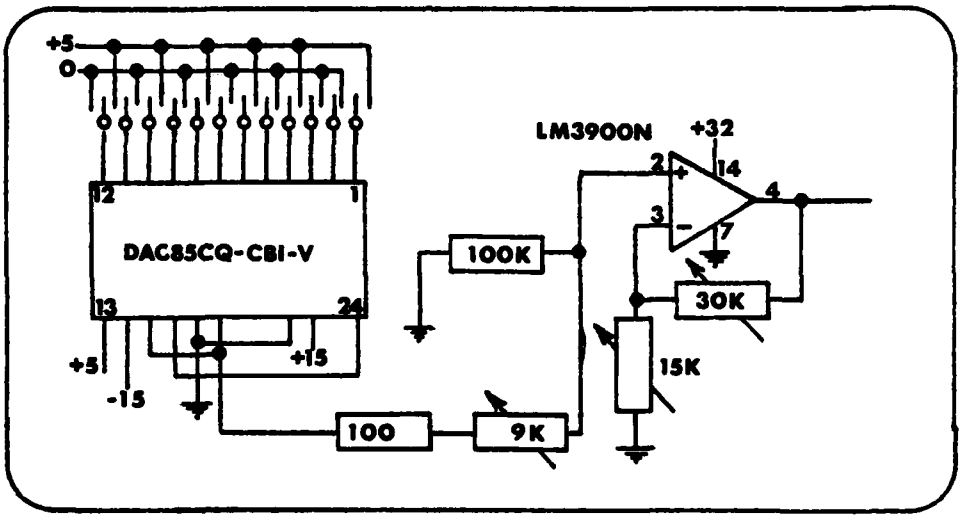


Fig. III-15 - D/A Converter / Op Amp Test Circuit.

Switches were used in the D/A converter input address lines so these lines could be programmed "high" or "low". This allowed simulation of binary addresses from the Intel 2716 EPROMs. Also, no high frequency capacitors were needed on the d.c. bias lines of the D/A converter because programming of the address lines was done manually.

The gain network of the op amp, consisting of the 15K ohm and 30K ohm resistors, was precisely adjusted by using trim pots instead of fixed-value resistors. Another trim pot, in series with the non-inverting input of the op amp, was used to adjust the op amp so it would not saturate

before the maximum voltage swing from the D/A converter was reached.

Since 12 address bits allow 4096 possible addresses, it was impractical to simulate each possible address as an input to the D/A converter. Instead, addresses were manually programmed at random in order to produce the expected 0 to +10 volt output swing of the D/A converter. Voltage measurements were taken at the output of the D/A converter (pin 15) and at the output of the op amp (pin 4). The actual gain profile of the op amp was obtained by plotting it's output voltage versus it's input voltage over the voltage input range. The expected gain of the amplifier was three, so the expected gain profile of the op amp over the input voltage range was calculated by multiplying the input voltage by this factor. Both of these curves are shown in Figure III-16 for comparison. The actual data is presented in tabular form in Appendix B.

Although the measured op amp gain was slightly less than the expected gain on the low end of the voltage input range, and slightly higher than the expected gain on the high end of the input voltage range, it was quite linear and agreed closely with the expected op amp gain. The actual op amp output voltage had a saturated value of 31.1 volts when the input voltage reached 9.91 volts. With an input of zero volts, the op amp had an output (offset) voltage of 0.48 volts.

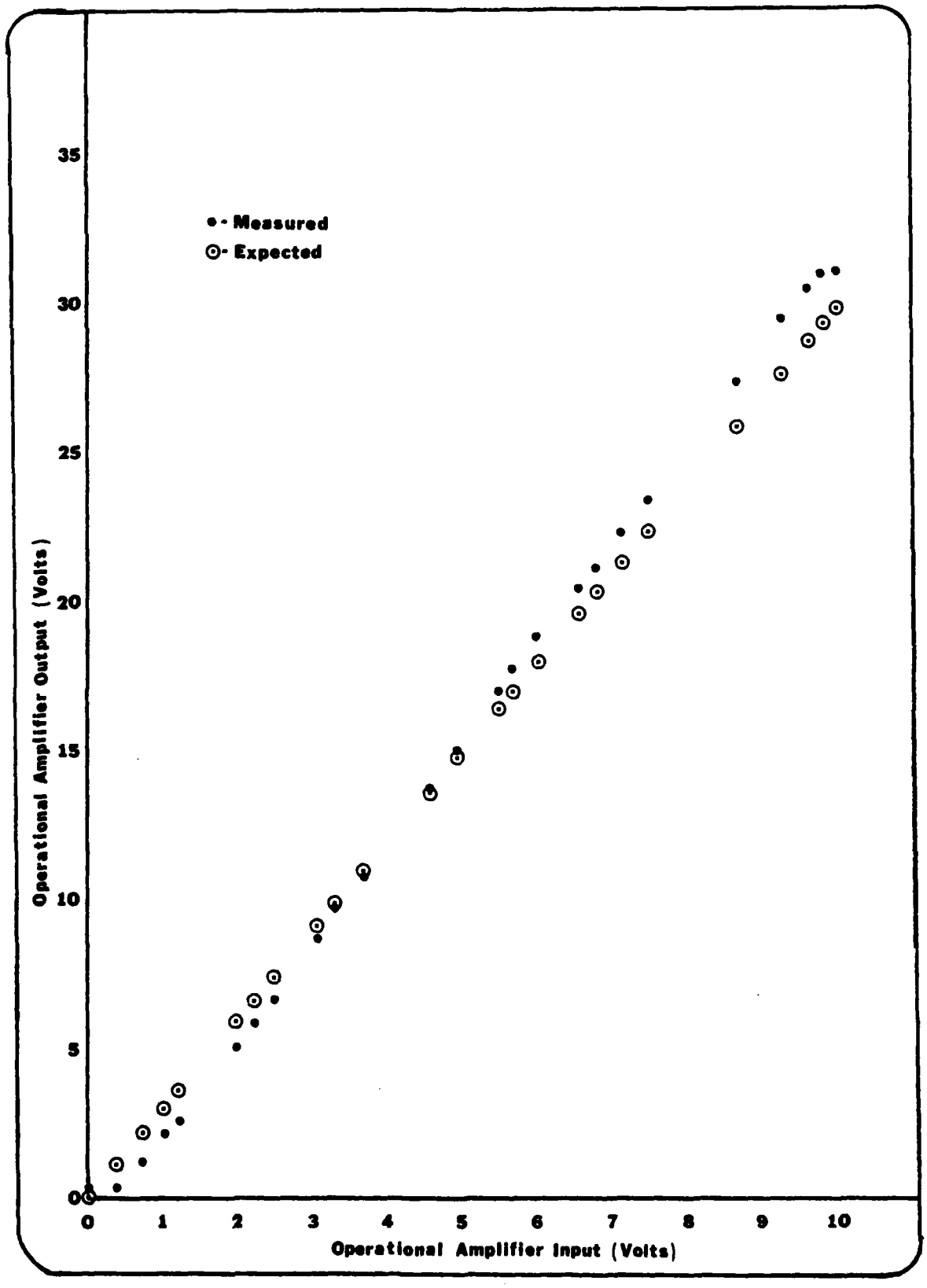


Fig. III-16 - Op Amp Actual/Expected Gain Profiles

Phase Shifter Test. In order to test the operation of the phase shifter circuit, a special circuit board was fabricated which contained the D/A converter, op amp circuit, and phase shifter. This circuit board is shown in Figure III-17. A Hewlett Packard 8410A network analyzer with a 8412A phase-magnitude display was used to monitor the output signal of the phase shifter. A baseline for the phase measurements was established by connecting a coaxial cable between the test ports of the network analyzer and observing the phase at 300 MHz. This became the "zero phase" point from which all other phase readings were referenced. Binary codes were programmed on the switches leading to the D/A converter input lines; and the output voltage of the op amp as well as the output signal of the phase shifter circuit were monitored. The data is presented in tabular form in Appendix C and plotted in Figure III-18. At the lowest setting, with an op amp output of 0.465 volts, the phase shift was 72 degrees at 300 MHz. The phase shift increased to a maximum of 179 degrees with 30 volts applied to the phase shifter input. This was a total change in phase shift of 107 degrees.

Combined RF and Feedback Circuitry.

The purpose of combining the RF and feedback circuitry was to verify proper operation of the thermometer and clock loops and to determine the amount of frequency shift which could be obtained from the phase shifter circuit.

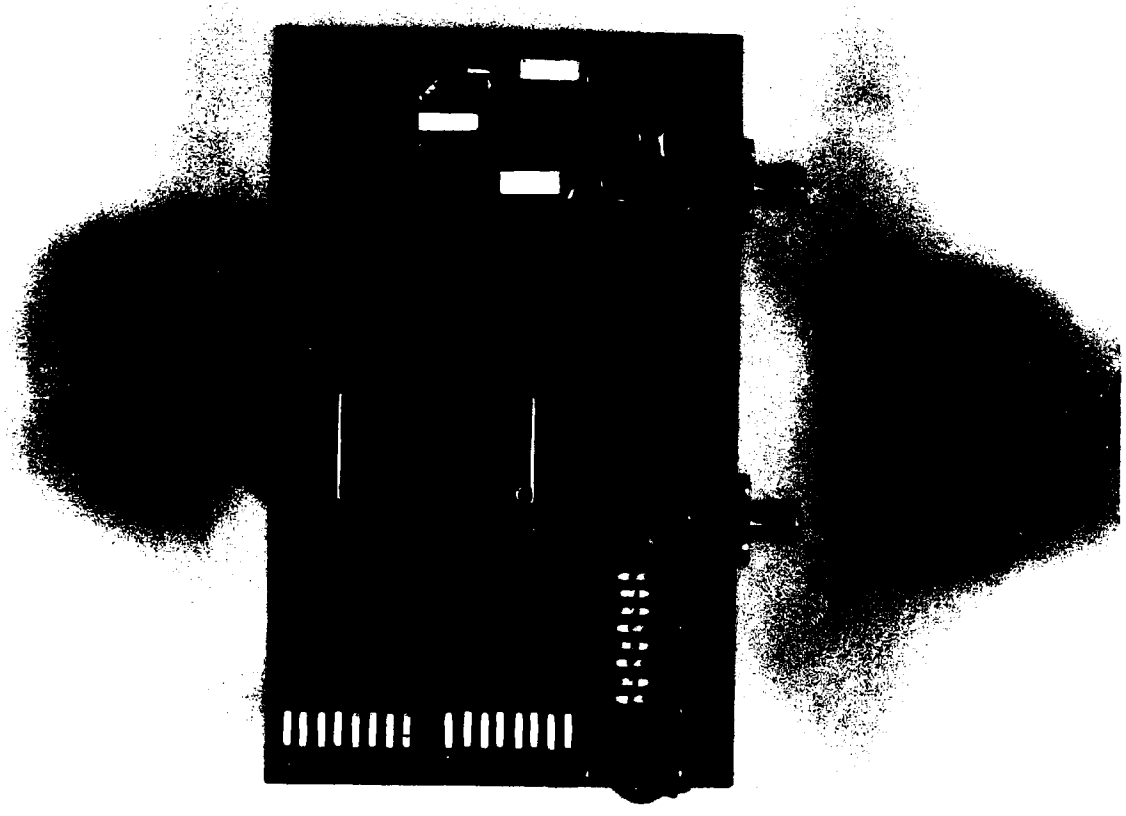


Fig. III-17 - Phase Shifter Test Circuit Board

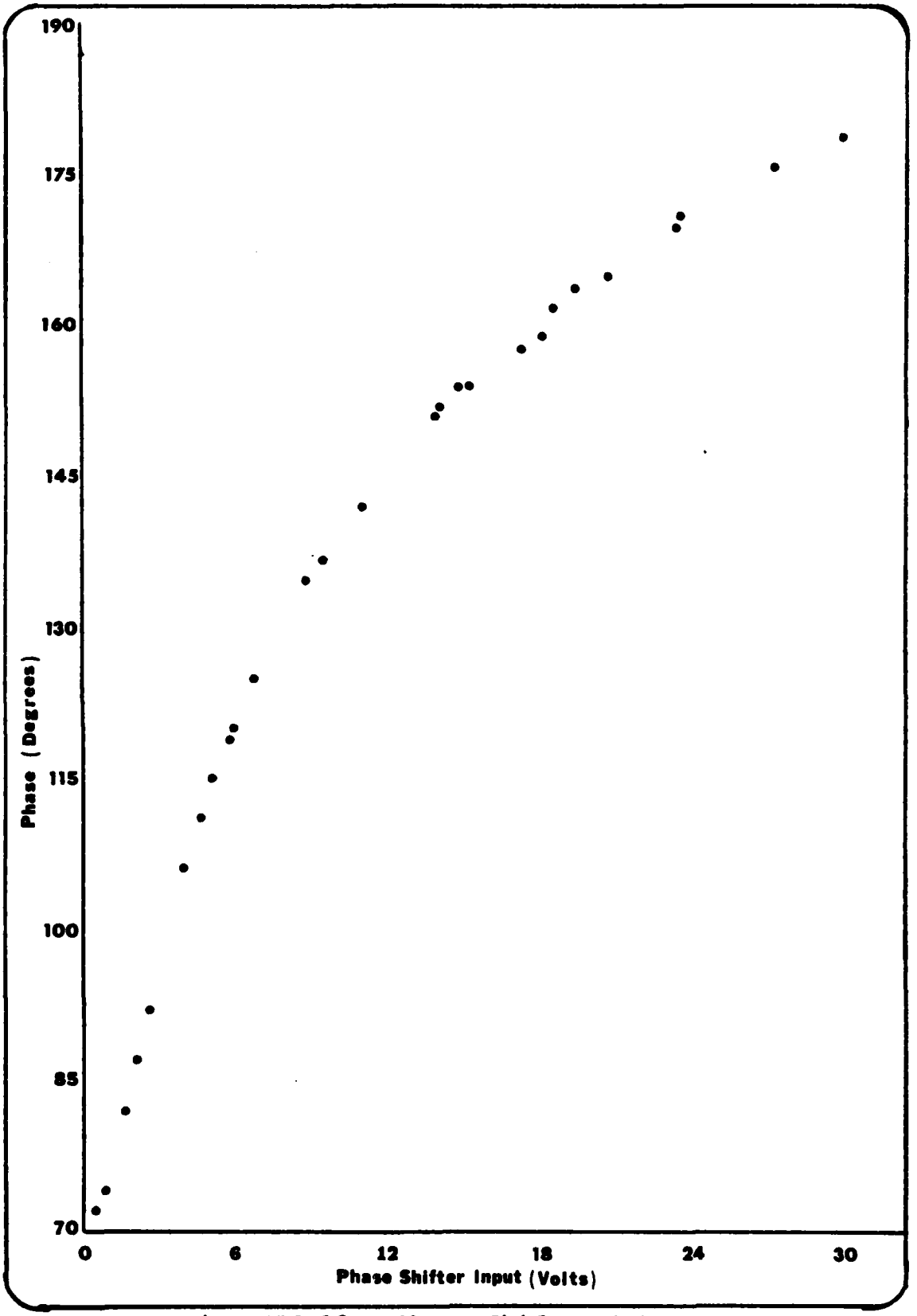


Fig. III-18 – Phase Shifter Output

Tuning the RF Feedback Loops. The purpose of tuning the RF feedback loops was to determine the amount of attenuation as well as phase shift needed in the thermometer and clock loops to cause the loop oscillation to lock on to the resonant frequency of the SAW paths. A prototype circuit board, similar to Figure II-9 and II-10, was fabricated for this purpose. The circuit board contained the SAW device, MICamps, couplers, and phase shifter circuit necessary for the two RF feedback loops to operate.

Thermometer Loop. Figure III-19 depicts the method used to tune the thermometer loop. The thermometer feedback loop was left open, and a sub-miniature adapter (SMA) was soldered on each side of the open transmission path. Power was applied to the MICamp, and a Cutler-Hammer 707 spectrum analyzer was used to observe the oscillating frequencies of the loop. Various lengths of coaxial cable along with several combinations of attenuators were inserted into the transmission path until an optimum combination was found that would cause the loop to oscilate at the SAW (path 3 to 4) resonant frequency. Through this trial and error process, it was found that a 29-inch length of cable combined with 9 dB of attenuation would satisfy the requirement for oscillation at the SAW resonant frequency of 309 MHz. Since 39-inches (1 meter) of cable represents a 360 degree phase shift, the phase shift represented by the cable was:

$$(29/39)(360^{o}) \simeq 270^{o}$$

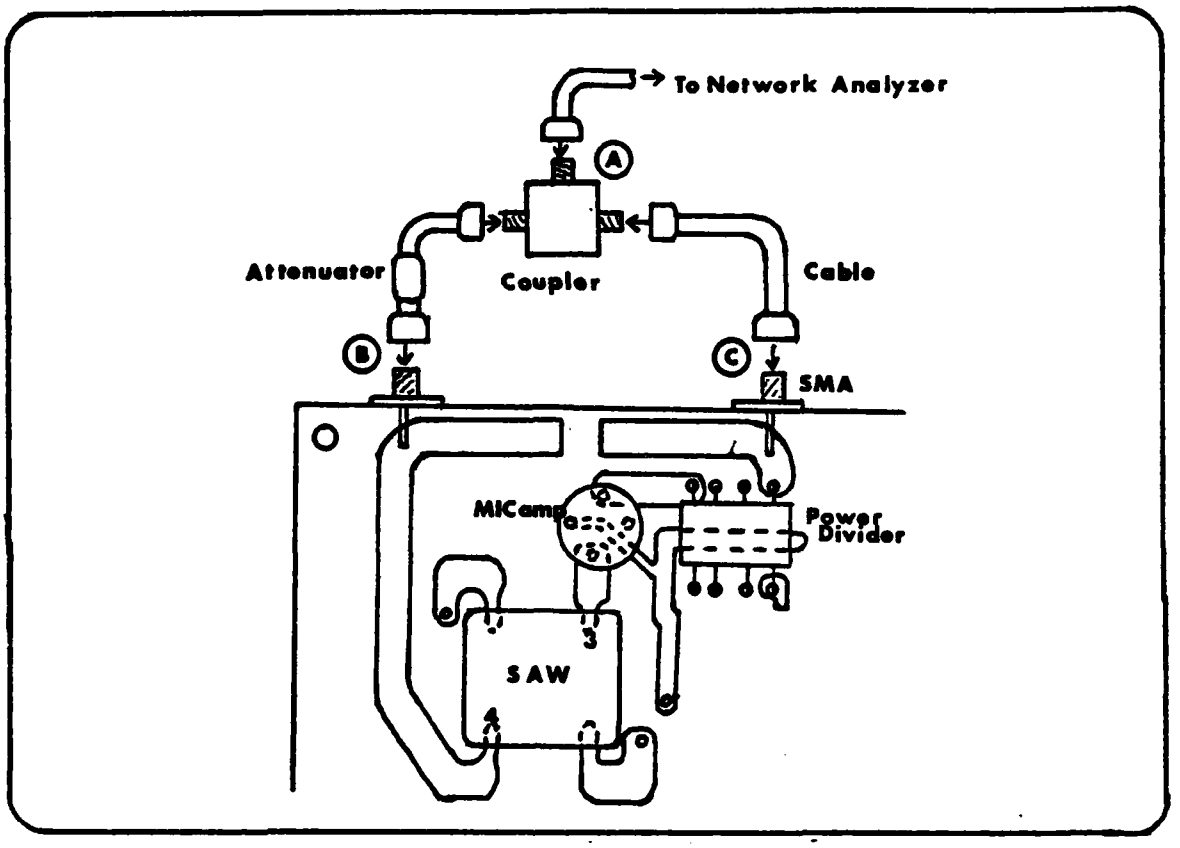


Fig. III-19 - Thermometer Loop Tuning Method.

Since 270 degrees is equivalent to -90 degrees, a 1000pf UHF capacitor was soldered into the transmission path in series with a 3 dB and a 6 dB attenuator. Subsequent re-testing of the thermometer loop showed that this combination caused the loop to oscillate at the SAW resonant frequency as expected. The thermometer loop resonant frequency of 309 MHz is shown in Figure III-20. The side lobe frequencies, from left to right, are: 1) 286 MHz, 2) 297 MHz, and 3) 320 MHz. The dotted line at the top of Figure III-20 represents 0 dBm. Since the scale is 10 dB

per major division and the coaxial cable to the spectrum analyzer had a 20 dB attenuator inserted, it can be seen that the oscillator power at test point C is +11 dBm.

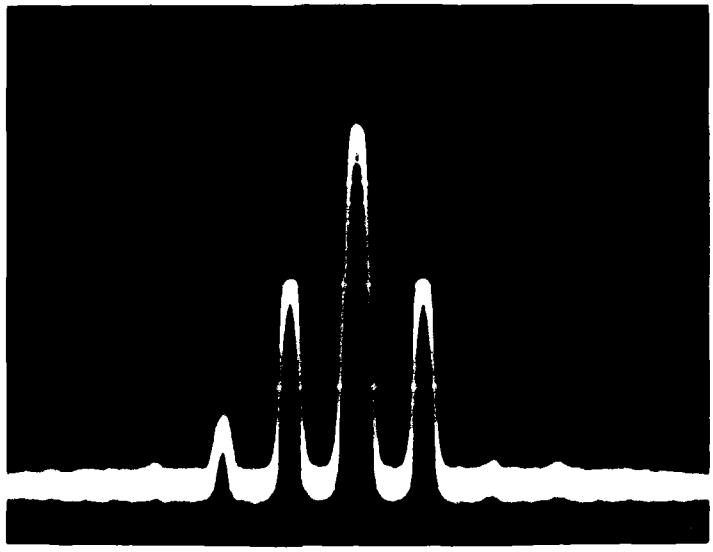


Fig. III-20 - Thermometer Loop Resonant Frequency.

Clock Loop. The procedure used for tuning the thermometer loop was also used for tuning the clock loop. This procedure is illustrated in Figure III-21. By trial and error, it was discovered that a 29-inch length of cable was also needed in the clock loop to cause oscillation at the SAW resonant frequency of 298 MHz. Additional attenuation caused the oscillation to lose lock, therefore none was used. A 1000pf UHF capacitor was inserted in the transmission path, and re-testing showed this to be adequate. The clock loop resonant frequency is shown in Figure III-22. The dotted line at the top of Figure III-22

represents 0 dBm. Since the scale is 10 dB per major division and the coaxial cable to the spectrum analyzer had a 20 dB attenuator inserted, the power in the loop is seen to be +9 dBm at 298 MHz. This is the amplitude of the RF output of the clock loop since the signal was measured at point A of Figure III-21. The side lobe frequencies, from left to right, are: 1) 265 MHz, 2) 286 MHz, 3) 309 MHz, 4) 320 MHz, 5) 330 MHz, and 6) 342 MHz.

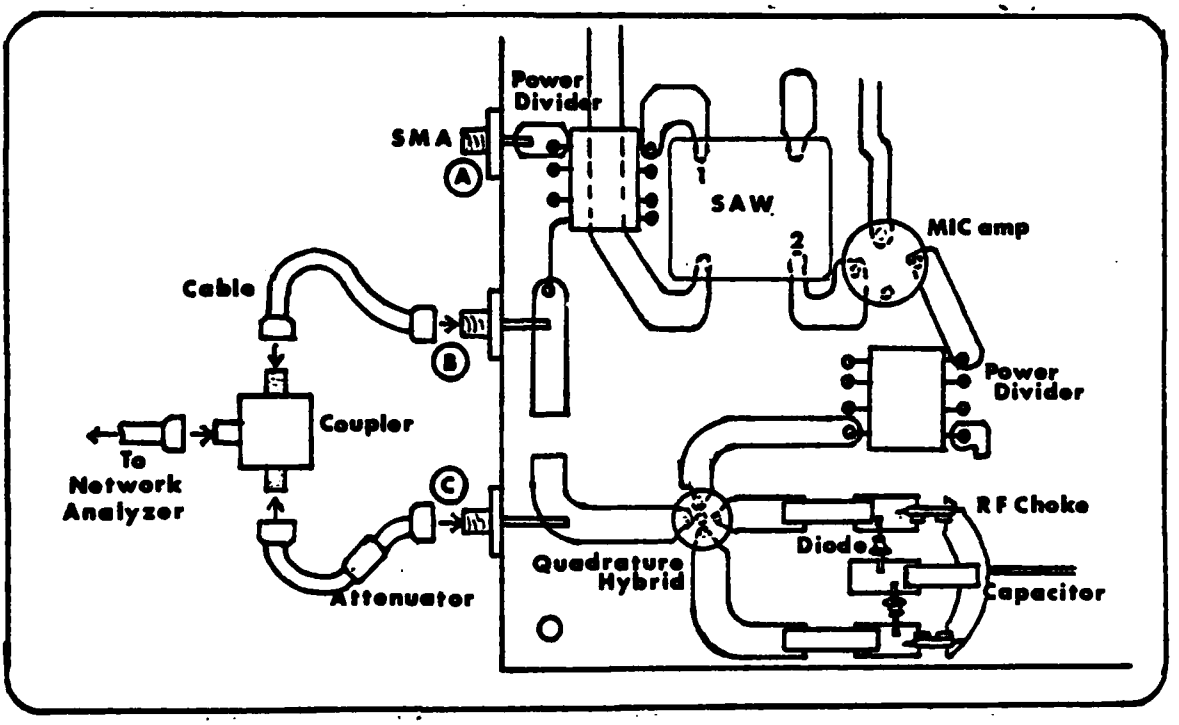


Fig. III-21 - Clock Loop Tuning Method.

Frequency Shift. With the RF loops tuned, the d.c. input voltage to the phase shifter was varied and the corresponding frequency reading of each loop was measured

using a Hewlett Packard 5340A frequency counter. The results are tabulated in Appendix D. From the data, it was obvious that the clock frequency could be varied from 298.6615 MHz to 298.8722 MHz. This is a frequency change of 210.7 KHz.

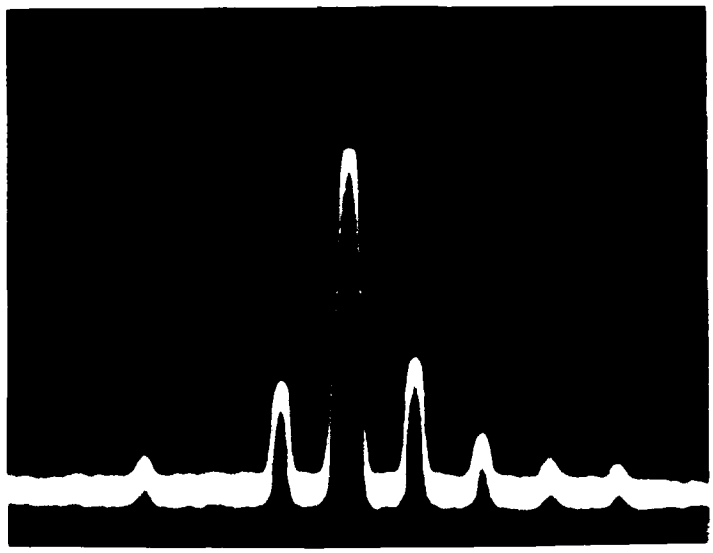


Fig. III-22 - Clock Loop Resonant Frequency.

Although the thermometer loop was supposed to be insensitive to frequency changes introduced by the phase shifter circuit, it was noticed that the thermometer frequency tended to rise and fall slightly with changes in the d.c. voltage applied to the phase shifter. The maximum frequency swing was approximately 7.6 KHz since the highest frequency recorded was 309.5935 MHz and the lowest frequency was 309.5859 MHz. The frequency shift is plotted in Figure III-23.

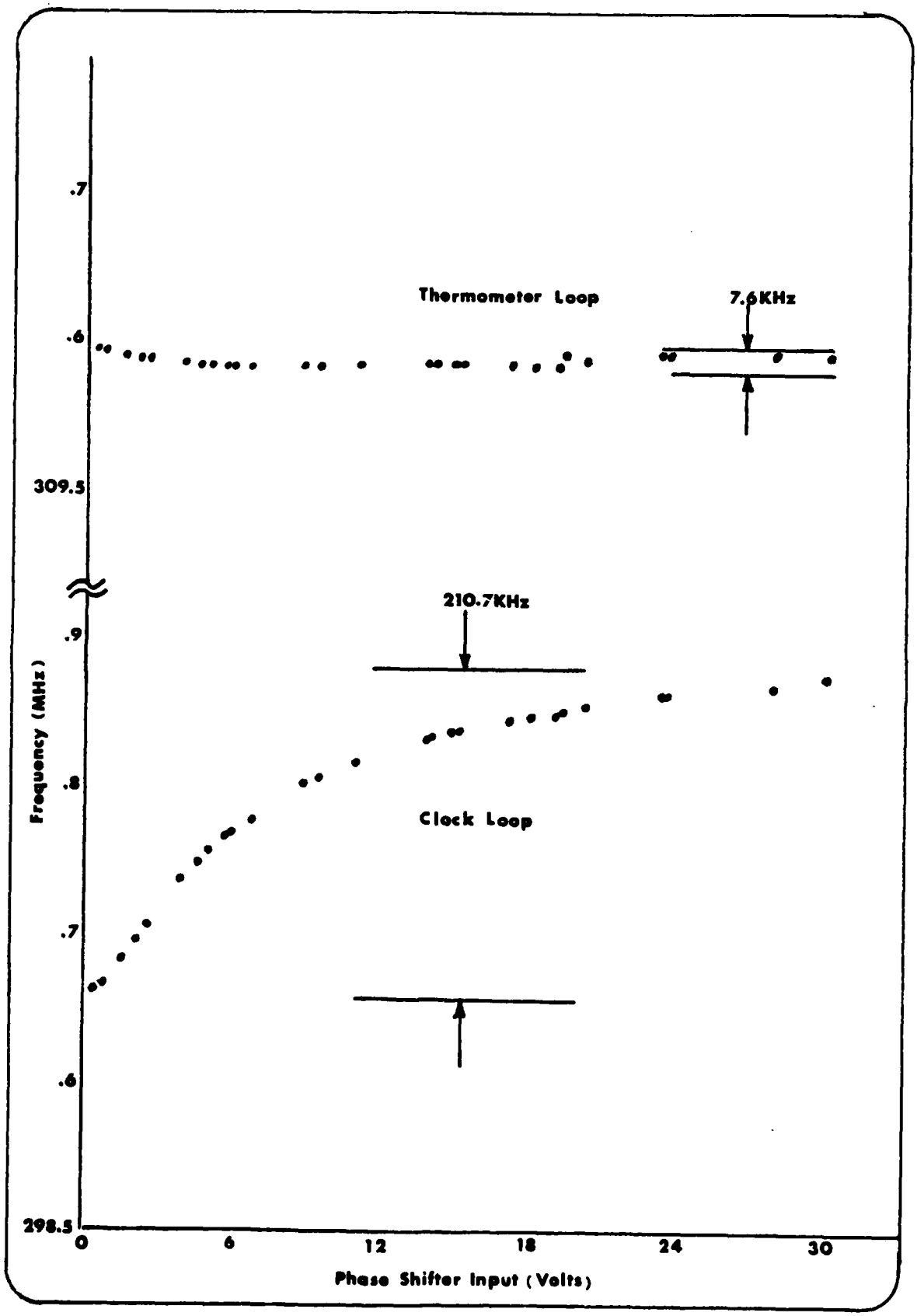


Fig. III-23. - Frequency Shift

IV. Conclusions and Recommendations

Conclusions.

Although this project did not progress to the point of obtaining a temperature stabilized SAW oscillator output, several accomplishments can be cited.

1. The SAW thermometer and clock loop designs were shown to be sufficient to cause resonant oscillation in both SAW paths. The thermometer path resonant frequency was 309 MHz. The clock path resonant frequency was 298 MHz, and the power at the RF output of this path was 9 dBm.

2. The D/A converter and op amp circuit was shown to operate as designed. A voltage swing of 0.5 volts to 30 volts was obtained from this design. Although the gain of the op amp was not always three, it was still quite linear and agreed closely with the expected gain.

3. The phase shifter circuit was verified as producing 107 degrees of phase shift over the 0.5 to 30 volt swing of its input. This was slightly less than the design value of 180 degrees of shift, but the amount of shift obtained is thought to be adequate for this project. Performance of the phase shifter may have been slightly degraded for a couple of reasons. The two varactor diodes used in the circuit may not have been as closely matched as they needed to be. Also, the phase quadrature of the QHT-2 coupler may have been a little "out of spec". Perfcrmance

AD-A138 313 SINGLE CIRCUIT BOARD IMPLEMENTATION OF A DIGITALLY COMPENSATED SAW OSCILLATOR (DCSO)(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI.. 2/2

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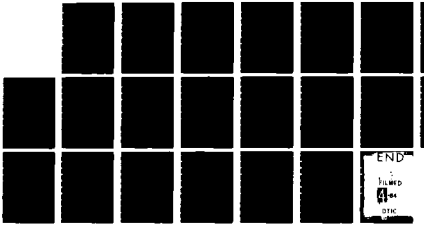
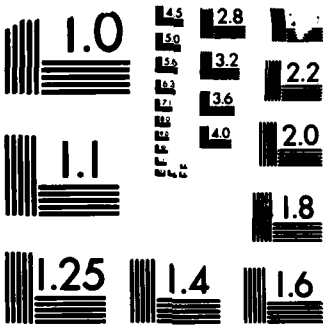




would also be degraded slightly if the impedance of the transmission lines was not exactly 50 ohms.

4. It was demonstrated that the clock loop frequency could be shifted from 298.6615 MHz to 298.8822 MHz, a range of 210.7 KHz. The thermometer loop was fairly insensitive (as expected) to frequency changes introduced by the phase shifter circuit; however, the thermometer loop frequency tended to rise and fall slightly with changes in the dc bias applied to the phase shifter. This total change was 7.6 KHz.

5. The AFIT IC chip was thoroughly tested, and its performance was found to be unsatisfactory. On twelve chips, the T-Chain operated below 330 Hz because there was a 2 msec lag between the time of the input signal to a TF stage and it's corresponding state change. This resulted in asymmetric signals instead of exactly divide-by-two signals at the DF latch outputs. The C-Chain suffered from the same type of problem except the asymmetry was even worse. The C-Chain did not produce an output signal at all on many of the twelve chips tested, and only one chip was suitable for testing of the C-Chain. The maximum operating frequency of the C-Chain was 600 Hz. The OM900 selector was tested on only two chips with the result that it appeared to be selecting the wrong input signals. Because the C-Chain stopped working on the one suitable chip, the control logic could not be verified completely.

6. The circuit board was fabricated by personnel at

the Avionics Laboratory and assembled, excluding the AFIT IC. Continuity of all the "runs" and connections was verified.

7. A package for the DCSO circuit board was designed. This package was fabricated by personnel at the AFIT model shop.

Recommendations.

Since most of the DCSO circuit has been shown to operate as designed, this thesis project should be continued. Specific recommendations are listed below.

1. Either of two things should be done concerning the AFIT IC chip. (a.) Investigate the reasons for the failure of the current CMOS/SOS design to function properly. This may include verifying the correctness of the metal pattern on the GUA. Possible defects in processing may have to be investigated; however, since the processing was done by a contractor, there is no control over this factor. Once the causes for failure have been discovered, a corrected version of the CMOS/SOS design should be resubmitted for fabrication. (b.) Investigate the possibility of implementing the AFIT IC using NMOS technology. This would require additional TTL prescaler circuitry since NMOS is much slower than CMOS. This additional TTL prescaler circuitry might be obtained in unpackaged chips which could be included in the AFIT IC package as shown in Figure IV-1. This packaging method is made necessary because there is no

additional room on the present DCSO circuit board for additional components.

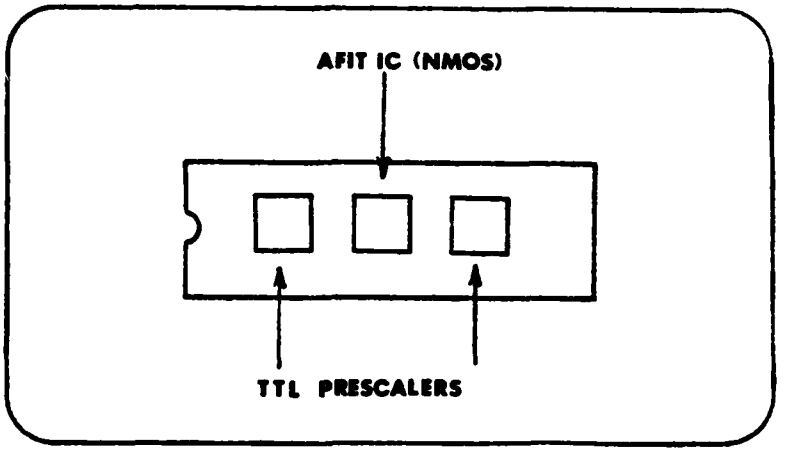


Figure IV-1 - Suggested AFIT IC package.

2. Power requirements for the present DCSO circuit are quite high. Calculations indicate approximately six watts are required. In effect, the DCSO circuit board in its package will be a small oven, and the heat generated may cause early failure of some of the components. The Avantek MICamps account for approximately two watts of the DCSO circuit power consumption. Therefore, an effort should be made to find MICamps which will require less power since the UTO-524 Micamps put out more power than is actually needed. In addition, other methods of dissipating the heat generated by the other circuit components should be investigated.

Bibliography

1. A-103/6-7. Designing with Modular Amplifiers. Product Catalog. Santa Clara, California: Avantek, 1979.

2. ATP-1035/9-76 Microwave Component Applications. Product Catalog. Santa Clara, California: Avantek, 1976.

3. Anzac Corporation. RF and Microwave Components, Anzac for the Next Generation. Product Catalog. Adams-Russell, 1982.

4. Burr-Brown Company. 1979 General Catalog. Product Catalog. Tucson, Arizona: Burr-Brown Co.,1979.

5. Inductive Components for Microelectronics Circuits. Product Catalog. Tyngsboro, Ma.: Piconics, Inc.

6. Intel Corporation. Intel Component Data Catalog. Product Catalog. 1980.

7. Lee, Donald L. "Design Considerations For Electronically Compensated SAW Delay Line Oscillators," IEEE Ultrasonics Symposium Proceedings, 79CH1482-9 :849-852 (1979).

8. Lindsey, Darryl. The Design and Drafting of Printed Circuits. Westlake Village, California: Bishop Graphics, Inc., 1979.

9. Linear Databook. Product Catalog. Santa Clara, California: National Semiconductor, 1978.

10. M-127. IF/RF Lumped Element Signal Processing Components. Product Catalog. West Caldwell, N. J.: Merrimac.

11. Microwave Varactor Diodes : Abrupt - Hyperabrupt. Specification Sheet. Woodside, N.Y.: MSI Electronics Inc.

12. Oliner, A. A., et al. Topics in Applied Physics, New York: Springer-Verlag (1978).

13. Pierce, J. F. and T. J. Paulus. Applied Electronics. Columbus: Charles E. Merrill Publishing Co., 1972.

14. Plessy Semiconductors. Integrated Circuits Databook. Product Catalog. Irvine, California: Oct. 1978.

15. Semiconductor Data Library Vol. 4 Series A. Product Catalog. U.S.A.: Motorola,Inc. (1974).

16. Sims, G. R., B. Varnum, N. Staubs, and P. Hall, "LSI

Implementation of a Digitally Compensated SAW Oscillator (DCSO) Controller Circuit," Final Report, School of Engineering, Air Force Institute of Technology (1982).

17. Slobodnik, A. J. "Surface Acoustic Waves and SAW Materials," IEEE Ultrasonics Symposium Proceedings, Vol. 64 No. 5:581-594 (May 1976).

18. Slobodnik, A. J., Jr., R. D. Colvin, G. A. Roberts, and J. H. Silva, Design and Test of a Digitally Compensated SAW Oscillator (DCSO), RADCTR81200, Hanscom AFB, MA. (1981).

19. Thin Film Chip Attenuators. Product Sheet. Whippany, New Jersey: KDI Pyrofilm Corp. (1979).

20. White, Joseph F., Semiconductor Control (Second edition). Massachusetts: Artec House, Inc., 1978.

Appendix A: Component Specifications

Anzac DS-109 Two-Way Power Divider (Ref. 3:204-205).

A power divider is ideally a lossless device which can also perform vector summation of two or more signals and thus is sometimes called a power combiner or summer. Power divider electrical parameters of principal importance to the designer and commonly specified by manufacturers are the following:

Frequency Range. This is the range over which specifications are guaranteed for the particular device.

Insertion Loss. The amount of attenuation, in excess of signal splitting losses, of an input signal from a source of chracteristic impedance Zo measured at an output port terminated in Zo.

Isolation. Isolation between two ports of a passive device is the amount of attenuation that a signal from a source of characteristic impedance Zo, applied to one port, undergoes when measured at the other port terminated in Zo.

Impedance. This is the nominal characteristic impedance (Zo) for the device.

VSWR. Voltage Standing Wave Ratio - VSWR is a measure of the impedance of a device relative to Zo. It can be expressed as VSWR = $(1+|\rho|)/(1-|\rho|)$ where $|\rho|$ is the magnitude of the reflection coefficient at the frequency of interest.

Amplitude Balance. This is the difference in attenuation between two or more output signals fed from a common input generally expressed as a maximum variation.

Phase Balance. This is the difference in phase between two or more output signals fed from a common input generally expressed as a maximum variation relative to the nominal phase difference between the paths. This nominal phase difference may be 0, 90, or 180 degrees.

Matched Power Rating (Input Power). This is the highest power level that can be applied to the input and still maintain other performance limits. It is stated with Zo terminations on all outputs to avoid reflected signals from unbalanced loads which may exceed the limit for power dissipation in the internal terminations.

Internal Load Dissipation. This is simply the power rating of any one of the internal terminations. The input power rating is normally several times larger than the internal load dissipation because most of the input power is

delivered to the output loads and not the internal terminations.

Specifications for the DS-109 Two-Way Power Divider are listed in Table A-1. The schematic diagram and mechanical data are shown in Figure A-1.

Table A-1

DS-109 Two-Way Power Divider Specifications

Frequency Range	10-500 Mhz
Insertion Loss	0.6 dB (max)
Isolation	25 dB (min)
Impedance	50 ohms (nominal)
VSWR	1.1 (typical midband)
Amplitude Balance	0.15 dB (max)
Phase Balance	1 degree (max)
Matched Power Rating	1 watt (max)
Internal load Dissipation	0.05 watt (max)

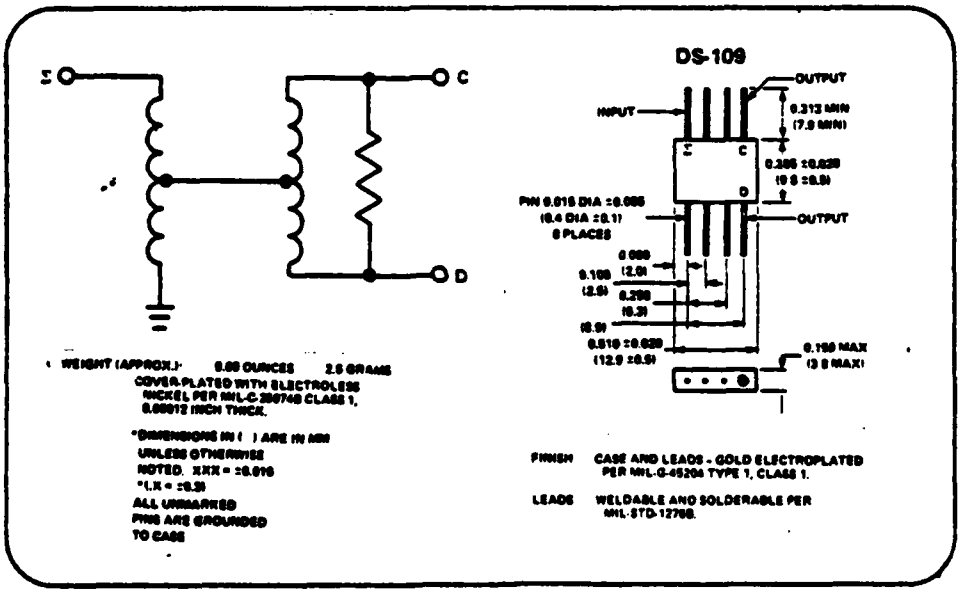


Fig. A-1 - Schematic Diagram/Mechanical Data. DS-109 Power Divider (Ref. 3:217).

Avantek UTO-524 MICamp (Ref. 1:1-2)

The UTO-524, housed in a TO-8T transistor package, provides a predictable, stable gain block suitable for a variety of amplifier applications. All that is needed is a 50 ohm microstrip environment with provisions for good grounding, a layout that isolates the input and output ports, a source of bias voltage and the UTO-524 will perform as well or better than its guaranteed specifications. The pin configuration for the UTO-524 is shown in Figure A-2.

The minimum frequency response of the UTO-524 is 5-500Mhz with a minimum gain of 30dB. Input power requirements are +15 volts at 70mA. The maximum noise figure is 4.0dB and the power output at the 1dB Gain Compression is +14dBm. The UTO-524 has a gain flatness of ± 1.0dB. The maximum Voltage Standing Wave Ratio (VSWR) is 2.0 for a 50 ohm load.

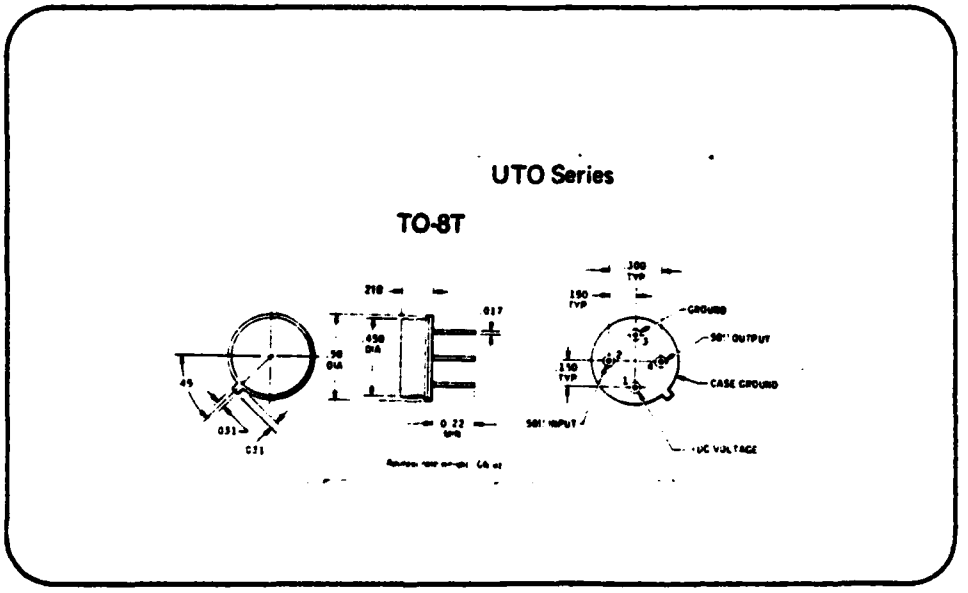


Fig. A-2 - UTO-524 MICamp Pin Configuration (Ref. 2:61).

Plessy SP8735B High Speed Divider (Ref. 14:173-175).

The SP8735B is a divide-by-eight circuit with a binary output. It is designed for operation from dc up to specified frequencies of 600Mhz over a temperature range of 0 to +70 degrees celcius.

This device, optimized for counter applications in systems using both Emitter Coupled Logic (ECL) and Transistor Transistor Logic (TTL), is intended to be operated between 0 volts and -5.2 volts and to interface with TTL operating between 0 volts and +5 volts. The binary outputs and one of two carry outputs are TTL-compatible, while the secondary carry output is ECL-compatible. The clock input, which is normally capacitively coupled to the signal source, is gated by an ECL III/ECL 10K compatible input. The TTL-compatible reset forces the 0000 state regardless of the state of the other inputs. The pin configuration for the SP8735B is shown in Figure A-4. A more complete listing of the SP8735B electrical characteristics is provided in Table A-2.

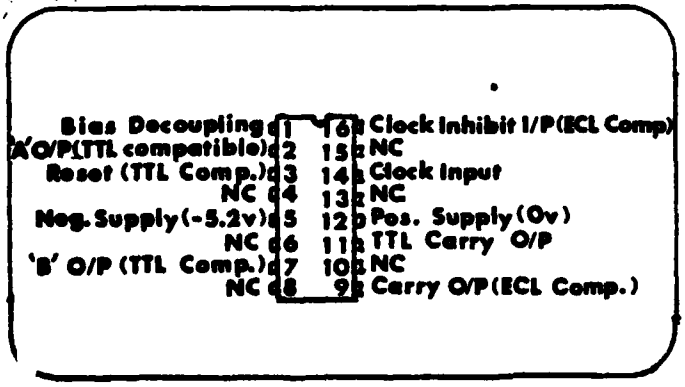


Fig. A-3 - Plessy SP8735B Pin Configuration. (Ref. 14:173).

Table A-2

Plessy SP8735B Electrical Characteristics (Ref. 14:174).

Test Conditions (unless otherwise stated):
T_{amb} 0°C to +70°C
Power Supplies V_{CC} 0V
V_{EE} −5.2V ±0.25V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock input (pin 14)					
Max. input frequency					
SP8735B	600			MHz	Input voltage 400–800mV p-p
SP8736B	500			MHz	
Min. input frequency with sinusoidal I/P			40	MHz	
Min. slew rate of square wave for correct operation down to DC			100	V/μs	
Clock inhibit input (pin 16)					
High level (inhibit)	−0.960			V	T_{amb} = +25°C (see note 1)
Low level			−1.650	V	
Edge speed for correct operation at max. clock I/P frequency			2.5	ns	10% to 90%
Reset input (pin 3)					
High level (reset)	See note 2				See note 2
Low level			+0.4	V	
Reset ON time	100			ns	
TTL outputs A & B (pins 2 & 7)					
Output high level	+2.4			V	10k Ω resistor and 3 TTL gate
Output low level			+0.4	V	from O/P to 5V rail (see note 3)
TTL carry output (pin 11)					
Output high level	+2.4			V	5k Ω resistor and 3 TTL gates from O/P to +5V rail
Output low level			+0.4	V	
ECL carry output (pin 9)					
Output high level	−0.975			V	T_{amb} = +25°C
Output low level			−1.375	V	External current = 0mA (See note 4)
Power supply drain current		70	90	mA	V_{EE} − 5.2V

NOTES

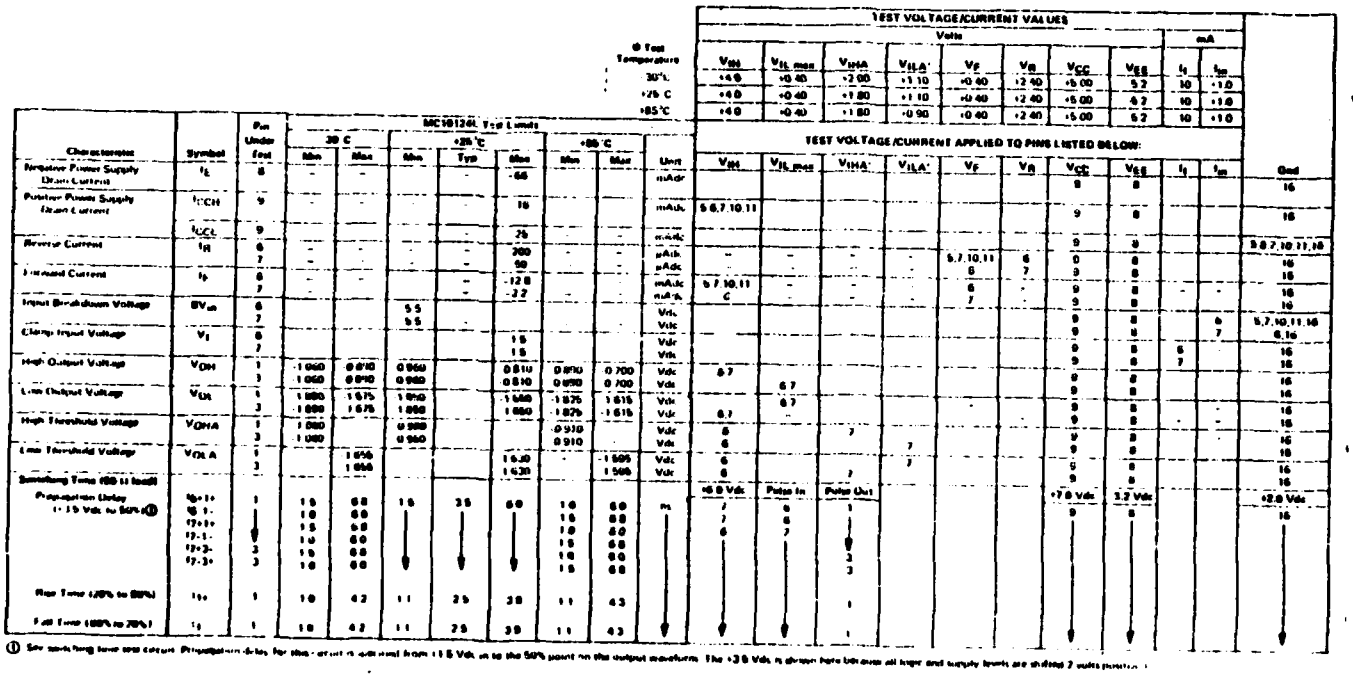
1. The clock inhibit input levels are compatible with the ECL III and ECL 10K levels throughout the temperature ranges specified.
2. For a high state, the reset input requires a more positive input level than the specified worst case TTL V_{OH} of −2.4V. Resetting should be done by connecting a 1.8k Ω resistor from the output of the driving TTL gate and only fanning out to the reset input of the SP8000 series devices.
3. These outputs are current sources which can be readily made TTL compatible voltages by connecting them to +5V via 10k Ω resistors (see Fig. 4).
4. The ECL carry output is compatible with ECL II throughout the temperature range but can be made compatible with ECL III using the simple interface shown in Fig. 3.

Motorola MC10124 Quad TTL-to-MECL Translator (Ref. 15:3-59).

Power supply requirements for the MC10124 are ground, +5.0 volts, and -5.2 volts. The dc levels are standard or

Table A-3

MC10124 Electrical Characteristics (Ref. 15:3-20)



Characteristic	Symbol	Pin Under Test	MC10124L Test Limits							Unit
			0°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Negative Power Supply Drain Current	I_E	8	-	-	-	-	-66			mAdc
Positive Power Supply Drain Current	I_{CCH}	9	-	-	-	-	16			mAdc
	I_{CCL}	9	-	-	-	-	25			mAdc
Reverse Current	I_R	6	-	-	-	-	200	-	-	µAdc
		7	-	-	-	-	50	-	-	µAdc
Forward Current	I_F	6	-	-	-	-	-128	-	-	mAdc
		7	-	-	-	-	-22	-	-	mAdc
Input Breakdown Voltage	BV_{in}	6			5.5					Vdc
		7			5.5					Vdc
Clamp Input Voltage	V_I	6					-1.5			Vdc
		7					-1.5			Vdc
High Output Voltage	V_{OH}	1	-1.060	-0.810	-0.960		-0.810	-0.890	-0.700	Vdc
		3	-1.060	-0.810	-0.960		-0.810	-0.890	-0.700	Vdc
Low Output Voltage	V_{OL}	1	-1.890	-1.675	-1.810		-1.650	-1.875	-1.615	Vdc
		3	-1.890	-1.675	-1.850		-1.650	-1.875	-1.615	Vdc
High Threshold Voltage	V_{OHA}	1	-1.080		-0.980			-0.910		Vdc
		3	-1.080		-0.960			-0.910		Vdc
Low Threshold Voltage	V_{OLA}	1		-1.656			-1.630	-	-1.595	Vdc
		3		-1.656			-1.630	-	-1.595	Vdc
Switching Times (50 Ω load)										
Propagation Delay (-1.3 Vdc to 50%) ①	t_{pd+}	-	1.0	6.0	1.5	3.5	6.0	1.0	6.0	ns
	t_{pd-}	-	1.0	6.0			6.0	1.0	6.0	
	t_{pd+}	-	1.0	6.0			6.0	1.0	6.0	
	t_{pd-}	-	1.0	6.0			6.0	1.0	6.0	
	t_{pd+}	3	1.0	6.0			6.0	1.0	6.0	
	t_{pd-}	3	1.0	6.0			6.0	1.0	6.0	
Rise Time (20% to 80%)	t_{tr}	1	1.0	4.2	1.1	2.5	3.8	1.1	4.3	
Fall Time (80% to 20%)	t_f	1	1.0	4.2	1.1	2.5	3.8	1.1	4.3	

TEST VOLTAGE/CURRENT VALUES											
Volts									mA		
V_{IH}	$V_{IL\ max}$	V_{IHA}	V_{ILA}	V_E	V_B	V_{CC}	V_{EE}	I_I	I_{in}	
+4.0	+0.40	+2.00	+1.10	+0.40	+2.40	+5.00	-5.2	10	+1.0	
+4.0	+0.40	+1.80	+1.10	+0.40	+2.40	+5.00	-5.2	10	+1.0	
+4.0	+0.40	+1.80	+0.90	+0.40	+2.40	+5.00	-5.2	10	+1.0	

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:										
V_{IH}	$V_{IL\ max}$	V_{IHA}	V_{ILA}	V_E	V_B	V_{CC}	V_{EE}	I_I	I_{in}	Gnd
						8	8			16
5,6,7,10,11						9	8			16
						9	8			5,6,7,10,11,16
				5,7,10,11	6	9	8			16
				6	7	9	8			16
5,7,10,11 C				6		9	8	-	-	16
				7		9	8			16
						9	8		6	5,7,10,11,16
						9	8		7	6,16
						9	8	6		16
						9	8	7		16
6,7						9	8			16
	6,7					9	8			16
	6,7					9	8			16
6,7	-			-	-	9	8	-	-	16
6		7				9	8			16
6			7			9	8			16
6		7				9	8			16
+6.0 Vdc	Pulse In	Pulse Out				+7.0 Vdc	-3.2 Vdc			+2.0 Vdc
7	6	1				9	8			16
7	6	1								
6	7	2								
		2								
		3								
		3								
		1								
		1								

① See switching time test circuit. Propagation delay for this circuit is measured from -1.3 Vdc on to the 50% point on the output waveform. The +3.0 Vdc is shown here between all logic and supply levels are shifted 2 volts positive.

Schottky TTL in and ECL 10K out. The internal schematic of this device is shown in Figure A-4. The electrical characteristics for the MC10124 are presented in Table A-3.

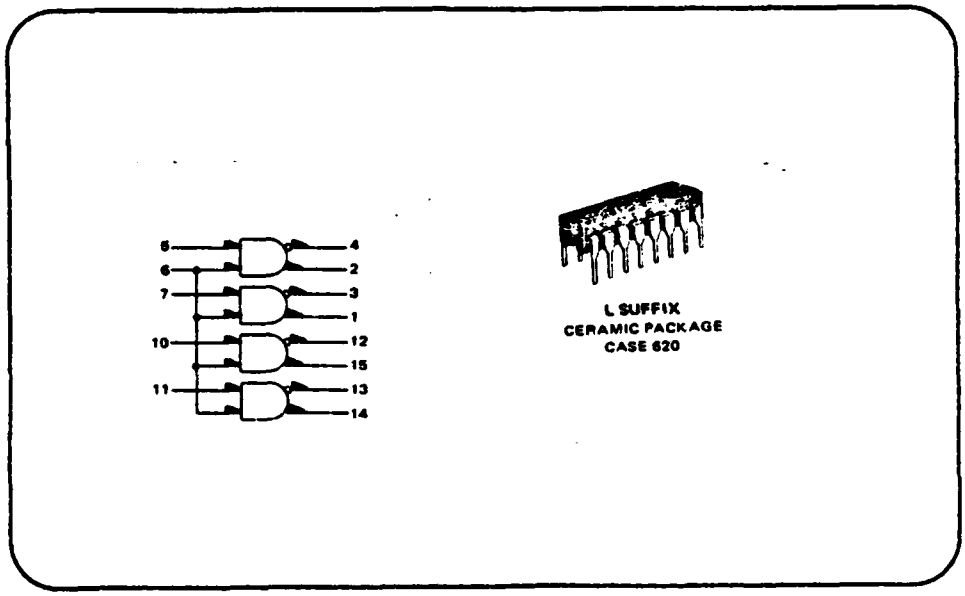


Fig. A-4 - MC10124 TTL-to-MECL Translator (Ref. 15:3-19).

Intel 2716 UV Erasable PROM (Ref. 6:2-7 - 2-10).

The Intel 2716 is a 16K (2K x 8) ultraviolet erasable and electrically programmable read-only memory which operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. The static standby mode reduces the power dissipation without increasing the access time. The maximum active power dissipation is 525mW while the maximum standby power dissipation is only 132mW.

The Intel 2716 uses single pulse TTL level programming which eliminates the need for high voltage pulsing. Any location can be programmed individually, sequentially, or at

random with the 2716's single address location programming. Total programming time for all 16,384 bits is 100 nanoseconds.

The pin configuration and block diagram of the Intel 2716 EPROM is shown in Figure A-5.

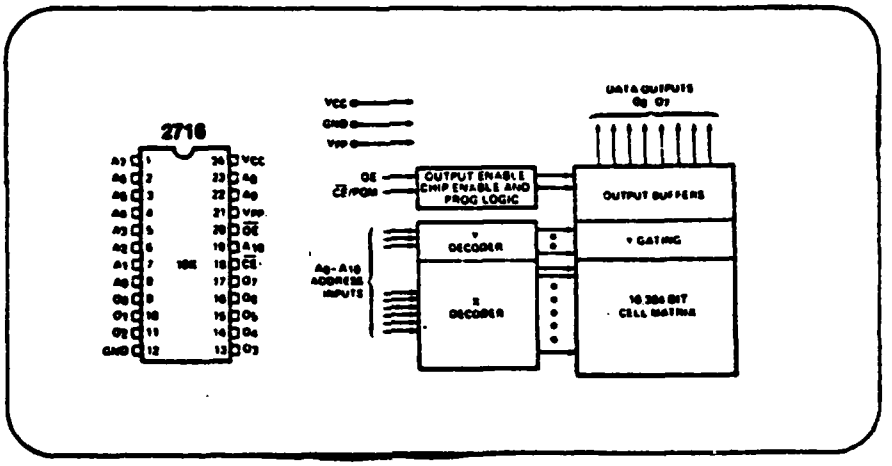


Fig. A-5 - Pin Configuration & Block Diagram. Intel 2716 EPROM (Ref. 6:2-7).

Burr-Brown DAC85CQ-CBI-V D/A Converter (Ref. 4:5-75 - 5-82).

The DAC85 is a 12 bit digital-to-analog converter which is housed in a 24 pin dual-in-line metal case. It is complete with an internal reference voltage and an output amplifier. The case is sealed for protection in rugged environments. Specifications of interest to the designer are discussed below.

Linearity. The linearity of a D/A converter is the true measure of its performance. The linearity error is specified over the entire operating temperature range of the D/A converter. The definition of this specification means

that the analog output will not vary by more than ±1 LSB from an ideal scraight line drawn between the end points (all bits on and all bits off) over the specified operating temperature range.

Differential Linearity. Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity specification of ± 1/2 LSB means that the output voltage can change anywhere from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next.

Gain Drift. Gain drift is a measure of the change in the full scale range analog output over temperature expressed in parts per million per degrees celcius (ppm/°C). The gain drift is determined by testing the end point differences at the lower and upper ends of the temperature range and calculating the GAIN ERROR with respect to the value at 25 degrees celcius and dividing by the temperature range.

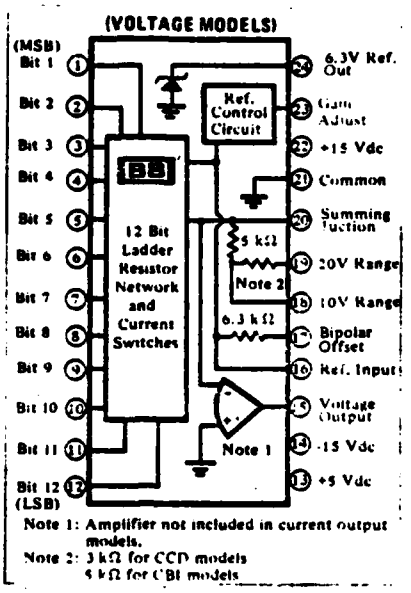
Offset Drift. Offset drift is a measure of the actual change in the output with all bits off over the specified temperature range. Output voltage measurements are taken at the lower and upper values of the specified temperature range. The maximum change in OFFSET is referenced to the

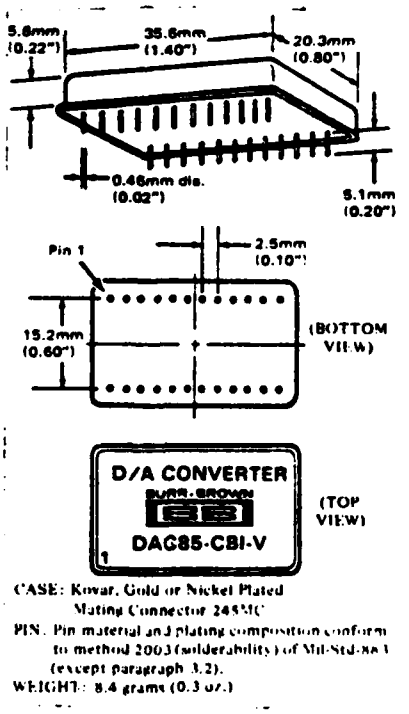
OFFSET at 25 degrees celcius divided by the temperature range. This drift is expressed in parts per million of full scale range per degree celcius (ppm FSR/°C).

Settling Time. The settling time is the total time (including slew time) for the output to settle to within an error band about its final value after a change in the input. Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20 volts and 10 volts and also for a 1 LSB change. The 1 LSB change is measured at the major carry (011111111111 to 100000000000) since this is the point where the worst case settling time occurs.

Power Supply Sensitivity. Power supply sensitivity is a measure of the effect of a power supply voltage change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the +15 volt or -15 volt and+5 volt power supplies about the nominal power supply voltages.

Specifications for the Burr-Brown DAC85 D/A converter are given in Table A-4. A more complete description as well as applications for the DAC85 can be found in Reference 4, pages 5-75 through 5-82. The connection diagram and mechanical data are given in Figure A-6.





CASE: Kovar, Gold or Nickel Plated
Mating Connector 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 8.4 grams (0.3 oz.)

Fig. A-6 - DAC85 Connection Diagram/Mechanical Data. (Ref. 4:5-76).

Table A-4
Burr-Brown DAC85CQ-CBI-V Specifications.
(Ref. 4:5-76).

Resolution	12 bits
Logic Levels (TTL Compatible)	
Logic "1"	+2v to +5.5v @ +40uA
Logic "0"	0v to +0.8v @ -1.0mA
Linearity Error @ 25 C (max)	±1/2 LSB
Differential Linearity Error	±1/2 LSB
Gain Error	±0.1%
Offset Error	±0.05% of FSR
Gain Drift	±20 ppm/°C
Offset Drift	±1 ppm of FSR/°C
Settling Time to ±0.01% of FSR	
for FSR change	
with 10 K-ohm feedback	5 usec
with 5 K-ohm feedback	3 usec
for 1 LSB change	1.5 usec
Slew Rate	20 V/usec
Voltage Ranges	±2.5v,±5v, ±10v,+5v,+10v
Output Current (min)	±5 mA
Output Impedance (dc)	0.05 ohms
Internal Reference Voltage	+6.3 volts
Power Supply Sensitivity	
+15 volt supply	+0.02% of FSR/%V
-15 and +5 volt supplies	±0.002% of FSR/%V
Power Supply Requirements	
Rated Voltage	±15 and +5 volts
Range	
±15 Volt Supply	+14.5v to ±15.5v
±5 Volt Supply	±4.75v to ±15.5v
Supply Drain	
±15 Volt Supply(5mA load)	±25 mA
±5 Volt Supply	±20 mA
Temperature Range	0 to +70 deg. C

Merrimac QHT-2 Coupler (Ref. 10:58).

The QHT-2 is a high performance, ultra-miniature quadrature hybrid coupler housed in a TO-5 case. The QHT-2 has a center frequency of 300Mhz and is designed for integration into transistor-type circuits because of its similarity of size and pin dimensions. The mechanical data for the QHT-2 is presented in Figure A-7, and the minimum

performance specifications are given in Table A-5.

Table A-5

QHT-2 Performance Specifications (Ref. 10:58).

Bandwidth	10%
Output Equality	0.6 dB
VSWR	1.2:1
Impedance	50 ohms
Isolation	25 dB
Coupling	-3 dB
Insertion Loss	0.2 dB
Phase Quadrature	90 deg. ±2 deg.
Power	250mW (average)
Weight	0.09 oz. (2.5 grams)

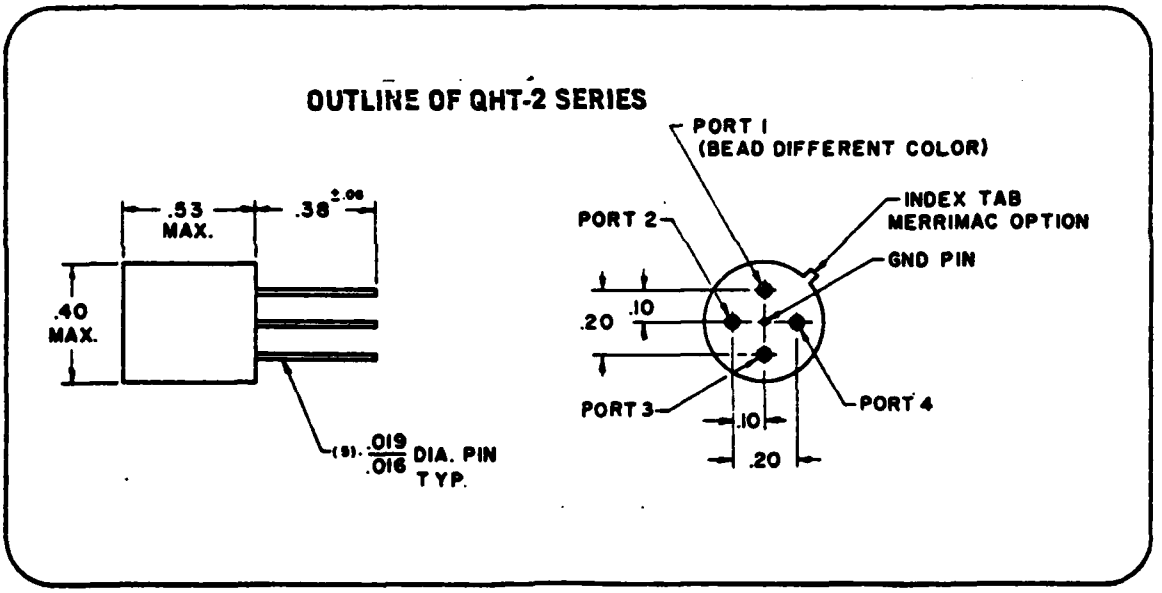


Figure A-7 - QHT-2 Mechanical Data (Ref. 10:58).

MSI HA1717F Varactor Diode (Ref. 11:12).

The HA1717F is a hyperabrupt microwave varactor diode with a 7.0:1 capacitance ratio. The capacitance at zero volts is 22 pf. The minimum reverse breakdown voltage is 30 V d.c. at a reverse voltage leakage current of 10 microamps d.c. The maximum reverse voltage leakage current is 0.02

microamps at a reverse breakdown voltage of 25 V d.c. and the minimum Q factor at 50 Mhz is 850. The dimensions for the HA1717F are given in Figure A-8.

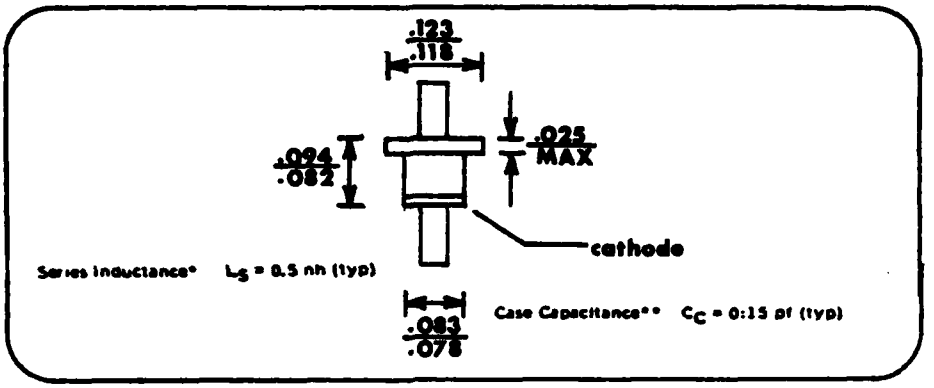


Fig. A-8 - HA1717F Mechanical Data (Ref. 11:12).

KDI Pyrofilm PCA3 and PCA6 Attenuators (Ref. 19:1).

The mechanical data for the PCA series of attenuators is shown in Figure A-9 and the specifications are presented in Table A-6. The PCA attenuator has an alumina substrate with solderable terminals constructed of silver plating over nickel.

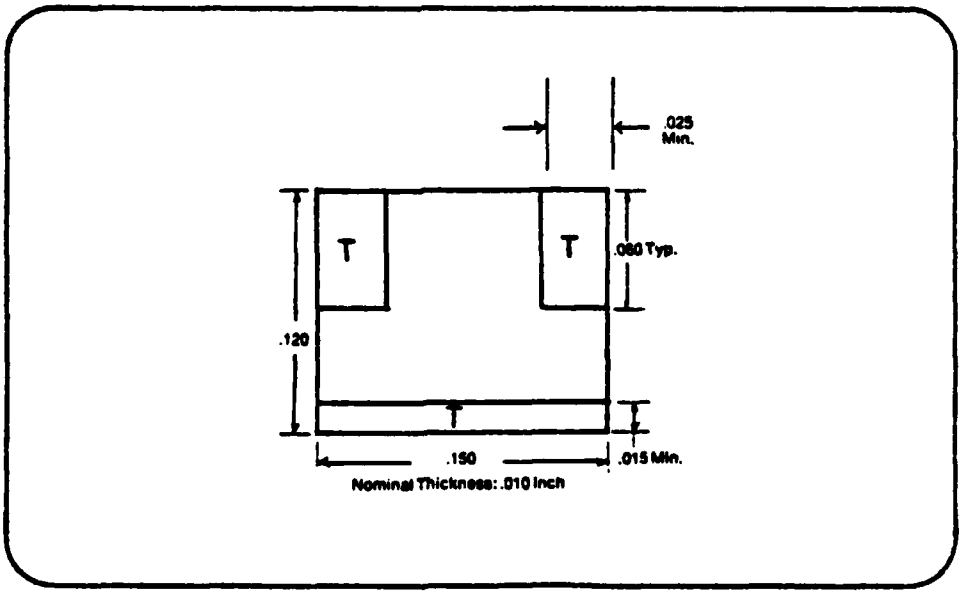


Fig. A-9 - PCA Attenuator Mechanical Data (Ref. 19:1).

Table A-6

PCA3 & PCA6 Attenuator Specifications (Ref. 19:1).

Attenuation	
PCA3	3 dB
PCA6	6 dB
Attenuation Sensitivity	±0.5 dB (D.C. to 12 GHz)
VSWR	
D.C. to 4 GHz	1.25
4 GHz to 8 GHz	1.35
8 GHz to 12 GHz	1.50
Operating Temperature	-55 to +150 deg. C
Impedance	50 ohms

Piconics PV471K81 Inductor (Ref. 5:8).

The mechanical data for the PV series of inductors is shown in Figure A-10 and the specifications are presented in Table A-7. The PV471K81 inductor has gold plated contact areas for bonding interconnecting leads. The bottom of the ceramic pad has a heavy gold plating for bonding the coil to a substrate.

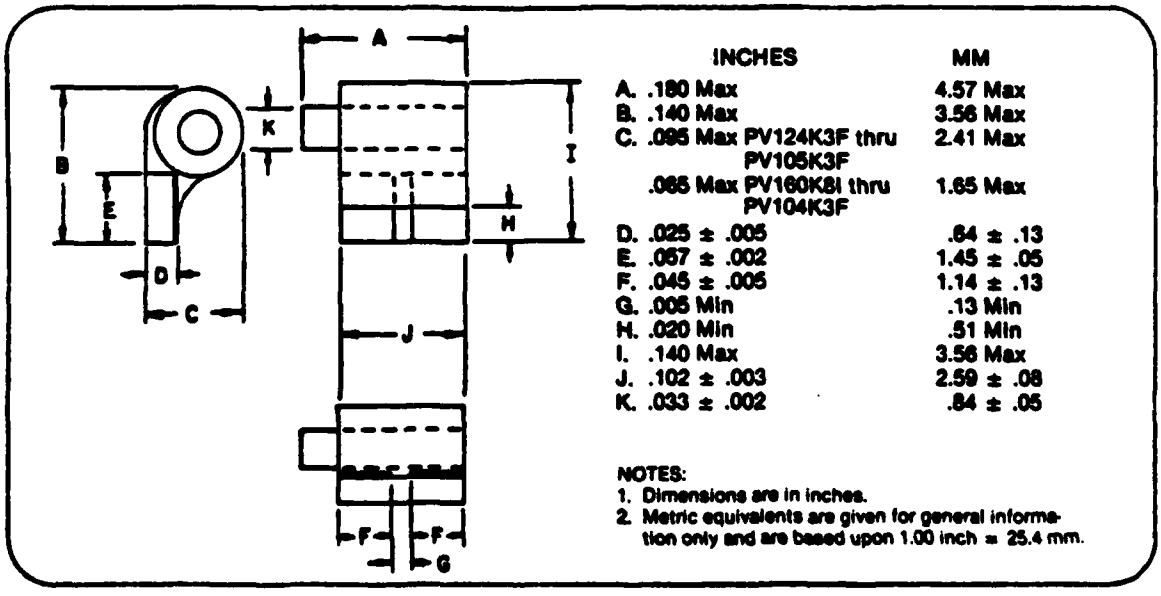


Fig. A-10 - PV471K81 Inductor Mechanical Data (Ref. 5:8).

Table A-7

PV Series Inductor Specifications (Ref. 5:8).

ELECTRICAL CHARACTERISTICS											
	Inductance			Q Min over L range	Q Typ at L Nom	Test Freq. 1/ MHz	SRF Min MHz	DC Res. at 25°C Max Ohms	2/ Current Max mA	Incremental Current mA 3/ Max
Part Number	Min µH	Nom µH	Max µH							
PV160K8I	.010	.013	.016	50	60	200	1200	.03	250	
PV250K8I	.018	.022	.025	50	60	200	1050	.07	250	
PV510K8I	.036	.044	.051	40	50	100	740	.13	250	
PV760K8I	.049	.065	.076	40	50	100	600	.20	250	
PV101K8I	.071	.085	.100	30	40	25	530	.32	250	
PV131K8I	.080	.105	.130	30	40	25	525	.34	200	
PV151K8I	.107	.129	.150	30	40	25	500	.35	200	
PV181K8I	.120	.150	.180	30	40	25	470	.41	180	
PV221K8I	.157	.189	.220	30	40	25	400	.45	180	
PV271K8I	.193	.232	.270	30	40	25	350	.50	180	
PV331K8I	.236	.283	.330	30	40	25	320	.60	140	
PV371K8I	.270	.300	.370	30	40	25	275	.62	140	
PV471K8I	.336	.403	.470	30	40	25	255	.65	100	
PV561K8I	.400	.480	.560	30	40	25	230	.75	100	
PV681K8I	.485	.583	.680	30	40	25	190	.85	100	
PV761K8I	.565	.660	.760	30	40	25	170	.88	100	
PV821K8I	.586	.703	.820	30	40	25	150	.90	100	
PV951K8I	.616	.783	.950	30	40	25	145	.95	100	
PV102K8I	.666	.833	1.00	25	35	7.9	140	.98	100	
PV152K8I	1.00	1.25	1.50	25	35	7.9	110	1.0	100	
PV222K8I	1.47	1.84	2.20	25	35	7.9	100	1.4	80	
PV272K8I	1.80	2.25	2.70	25	35	7.9	89	1.6	75	
PV332K8I	2.20	2.75	3.30	25	35	7.9	77	1.8	65	
PV472K8I	3.13	3.92	4.70	25	35	7.9	49	2.2	60	
PV562K8I	3.87	4.84	5.80	25	35	7.9	38	2.8	58	
PV682K8I	4.53	5.67	6.80	25	35	7.9	36	3.0	55	
PV822K8I	5.47	6.84	8.20	25	35	7.9	21	3.0	55	
PV103K3F	6.00	7.50	10.00	25	35	2.5	20	2.8	55	50
PV133K3F	6.50	9.75	13.00	25	35	2.5	19	3.0	53	45
PV163K3F	8.00	12.00	16.00	25	35	2.5	16	3.4	50	40
PV203K3F	10.00	15.00	20.00	25	35	2.5	14	3.5	43	37
PV223K3F	11.00	16.50	22.00	25	35	2.5	12	4.0	43	36
PV303K3F	15.00	22.50	30.00	25	35	2.5	11	4.5	40	32
PV383K3F	18.00	27.00	36.00	25	35	2.5	10	5.0	40	31
PV473K3F	23.00	35.00	47.00	25	35	2.5	6.5	5.7	39	29
PV563K3F	28.00	42.00	56.00	25	35	2.5	6.3	7.0	35	28
PV683K3F	34.00	51.00	68.00	25	35	2.5	6.2	8.0	30	28
PV753K3F	37.00	56.00	75.00	25	35	2.5	5.9	9.0	30	25
PV863K3F	43.00	65.00	86.00	25	35	2.5	5.6	10.0	28	23
PV104K3F	50.00	75.00	100	25	35	.79	5.3	12.0	27	20
PV124K3F	60.00	90.00	120	20	30	.79	4.4	14.0	25	20
PV154K3F	75.00	112.5	150	20	30	.79	4.0	18.0	22	20
PV474K3F	235	343	470	20	30	.79	2.1	30.0	16	16
PV684K3F	340	510	680	20	30	.79	2.1	35.0	15	15
PV105K3F	500	750	1 MH	20	30	.25	1.1	75.0	11	11

1/ Test frequency range: 0.25 MHz-25 MHz. Inductance should be measured on instruments such as the HP280-A Q Meter, HP4342A, HP250B RX Meter, or equivalent with TF-301 test fixture or equal. Fixture inductance and residual Q-Meter inductance should be subtracted from indicated inductance.
Test frequency range: 25 MHz thru 200 MHz. Inductance should be measured on instruments such as the HP160-A Q Meter, HP280-A Q Meter, HP4342A, HP250B RX Meter, or equivalent with TF-301 test fixture or equal. Fixture inductance should be subtracted from calculated inductance.
2/ Current required to not exceed specified temperature use.
3/ Applicable to ferrite core only.

ABSOLUTE MAXIMUM RATINGS

Operating temperature range: −55° to +125°C.
Storage temperature range: −55° to +125°C.
Temperature rise (at 90°C): 35°C.
Maximum operating temperature: 125°C.
Altitude: 70,000 feet.
Dielectric withstanding voltage: Method 301 of MIL-STD-202, test voltage 700 volts rms.
Barometric pressure: Method 105, test condition C. MIL-STD-202, (70,000 feet), test voltage 200 volts rms.

Appendix B: D/A Converter / Op Amp Test Data

D/A Converter Input (Binary)	D/A Converter Output (Volts)	Measured Op Amp Output (Volts)	Expected Op Amp Output (Volts)
000000000000	9.98	31.1	29.94
000000001000	9.97	31.1	29.91
000000010000	9.95	31.1	29.85
000000100000	9.91	31.1	29.73
000001000000	9.83	31.0	29.49
000010000000	9.65	30.5	28.95
000100000000	9.31	29.5	27.93
001000000000	8.68	27.4	26.04
001111111111	7.49	23.3	22.47
010000100001	7.15	22.3	21.45
010111111110	6.82	21.2	20.46
010101010101	6.60	20.5	19.80
011000100001	5.99	18.86	17.97
011010100001	5.68	17.83	17.04
011011111110	5.56	17.07	16.68
011111111110	4.96	15.00	14.88
100000000000	4.93	14.98	14.79
100000011111	4.86	14.73	14.58
100000100001	4.66	14.06	13.98
100010001110	4.58	13.83	13.74
100011100001	4.39	13.15	13.17
100010100001	4.36	13.02	13.08
101000000000	3.68	10.84	11.04
101010101010	3.29	9.47	9.87
101010111111	3.26	9.30	9.78
101011111111	3.12	8.79	9.36
101111111111	2.50	6.73	7.50
110001100011	2.25	5.92	6.75
110001100111	2.24	5.89	6.72
110001101111	2.22	5.83	6.66
110001111111	2.18	5.70	6.54
110010001110	2.14	5.57	6.42
110011001100	1.99	5.08	5.97
110011111111	1.87	4.65	5.61
110101010101	1.66	4.00	4.98
110111111111	1.25	2.66	3.75
111000111000	1.108	2.22	3.324
111001111111	0.935	1.676	2.805
111010101110	0.898	1.557	2.694
111011000000	0.777	1.193	2.331
111011100111	0.682	0.924	2.046

111011101110	0.664	0.878	1.992
111011111111	0.623	0.780	1.239
111111010101	0.101	0.480	0.303
111111110101	0.023	0.480	0.069
111111111101	0.004	0.480	0.012
111111111111	0.000	0.480	0.000

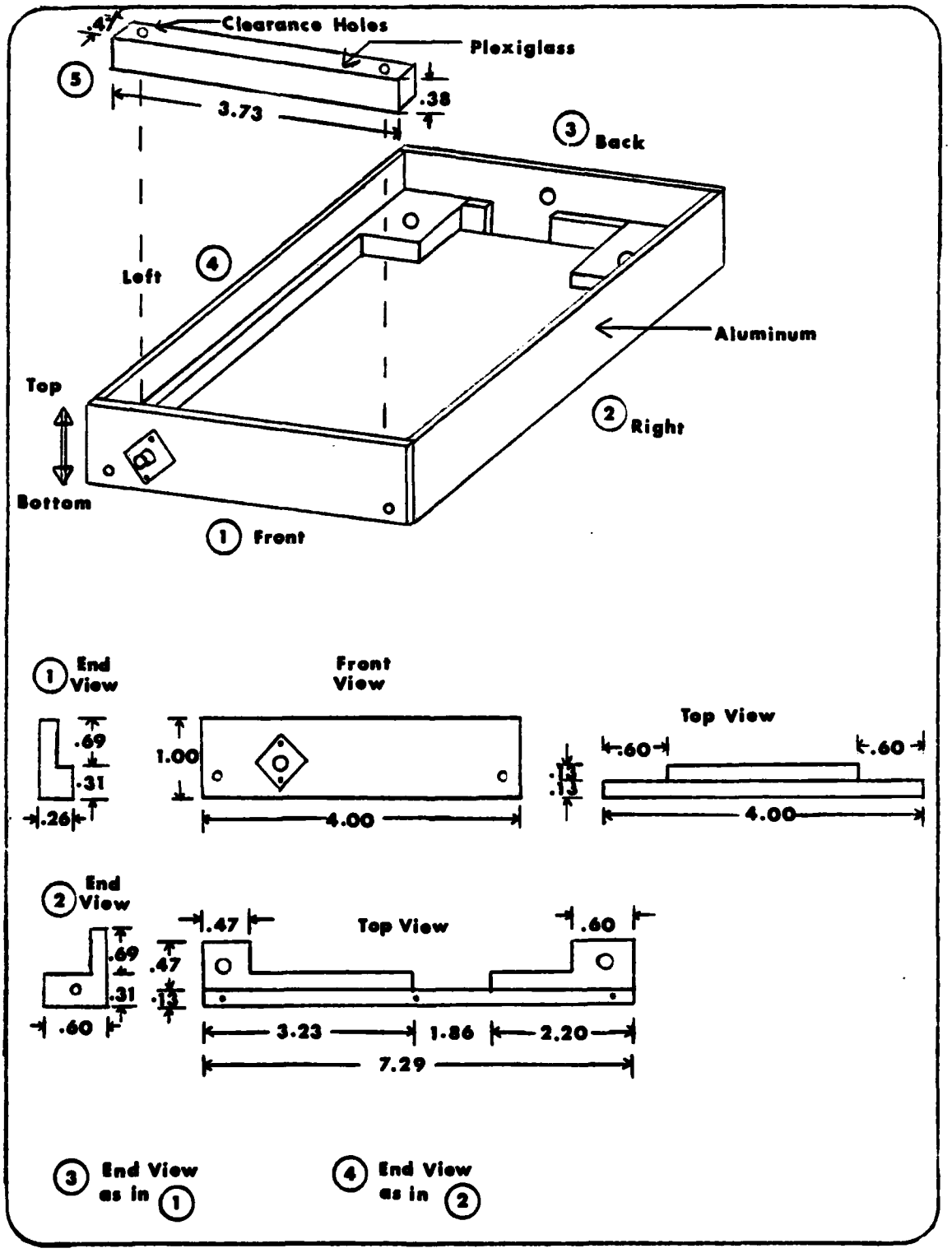
Appendix C: Phase Shift Data

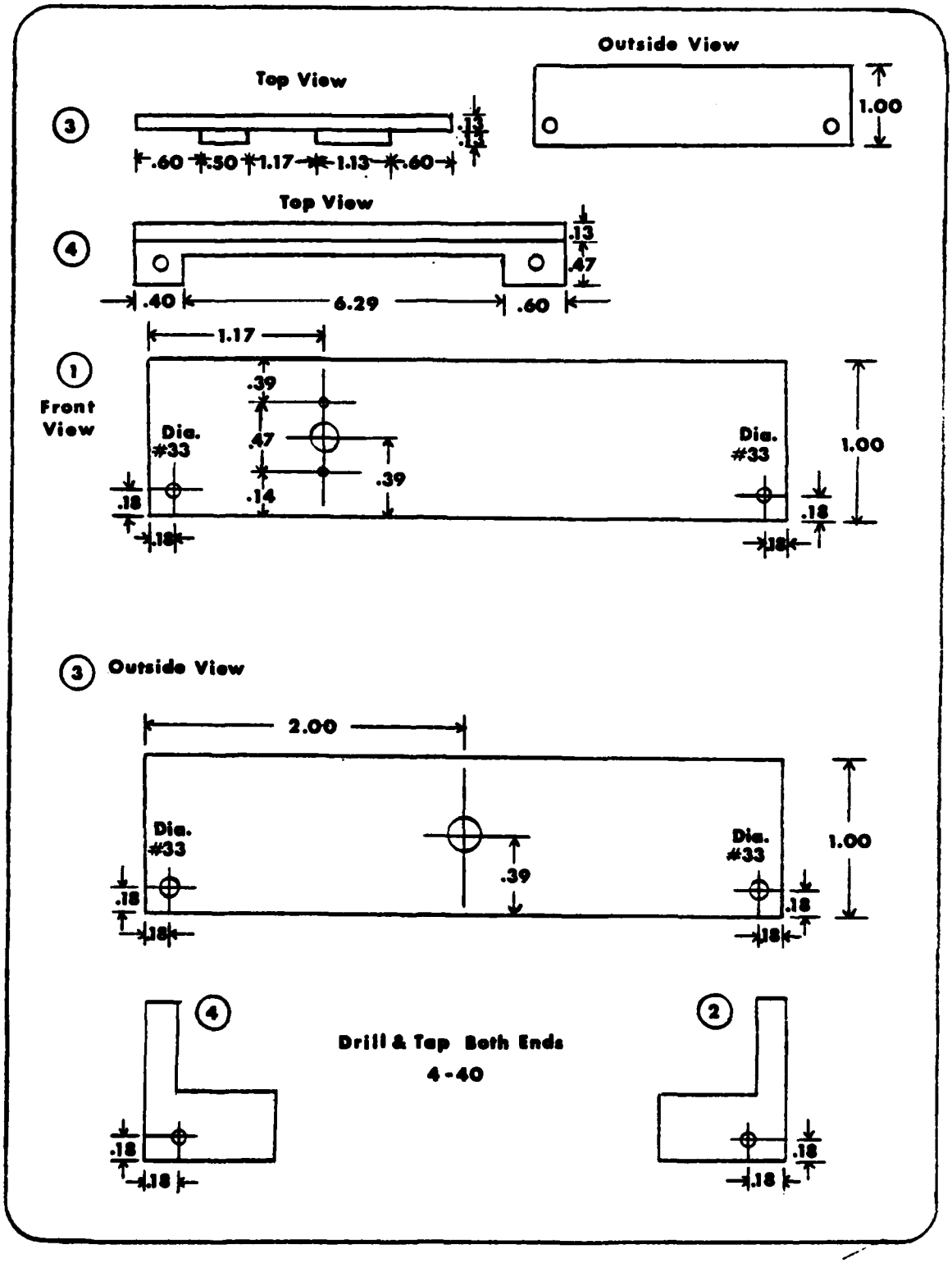
D/A Converter Input (Binary)	Measured OP Amp Output (Volts)	Insertion Loss (dB)	Measured Phase (Degrees)
111111111111	0.465	1.0	72.0
111011100111	0.836	1.0	74.0
111001111111	1.572	1.0	82.0
111000111000	2.12	1.0	87.0
110111111111	2.57	1.0	92.0
110101010101	3.93	1.0	106.0
110011111111	4.63	1.0	111.0
110011001100	5.04	1.0	115.0
110001111111	5.67	1.0	119.0
110001100011	5.90	1.0	120.0
101111111111	6.72	1.0	125.0
101011111111	8.83	1.0	135.0
101010101010	9.53	1.0	137.0
101000000000	10.93	1.0	142.0
100010100001	13.82	0.9	151.0
100010001110	13.98	0.9	152.0
100000011111	14.90	0.9	154.0
011111111110	15.17	0.9	154.0
011011111110	17.29	0.8	158.0
011010100001	18.06	0.8	159.0
011000100001	19.12	0.8	162.0
010111111110	19.40	0.8	164.0
010101010101	20.8	0.8	165.0
010000100001	23.4	0.8	170.0
001111111111	23.6	0.8	171.0
001000000000	27.9	0.8	176.0
000100000000	30.0	0.8	179.0
000010000000	30.1	0.8	179.0

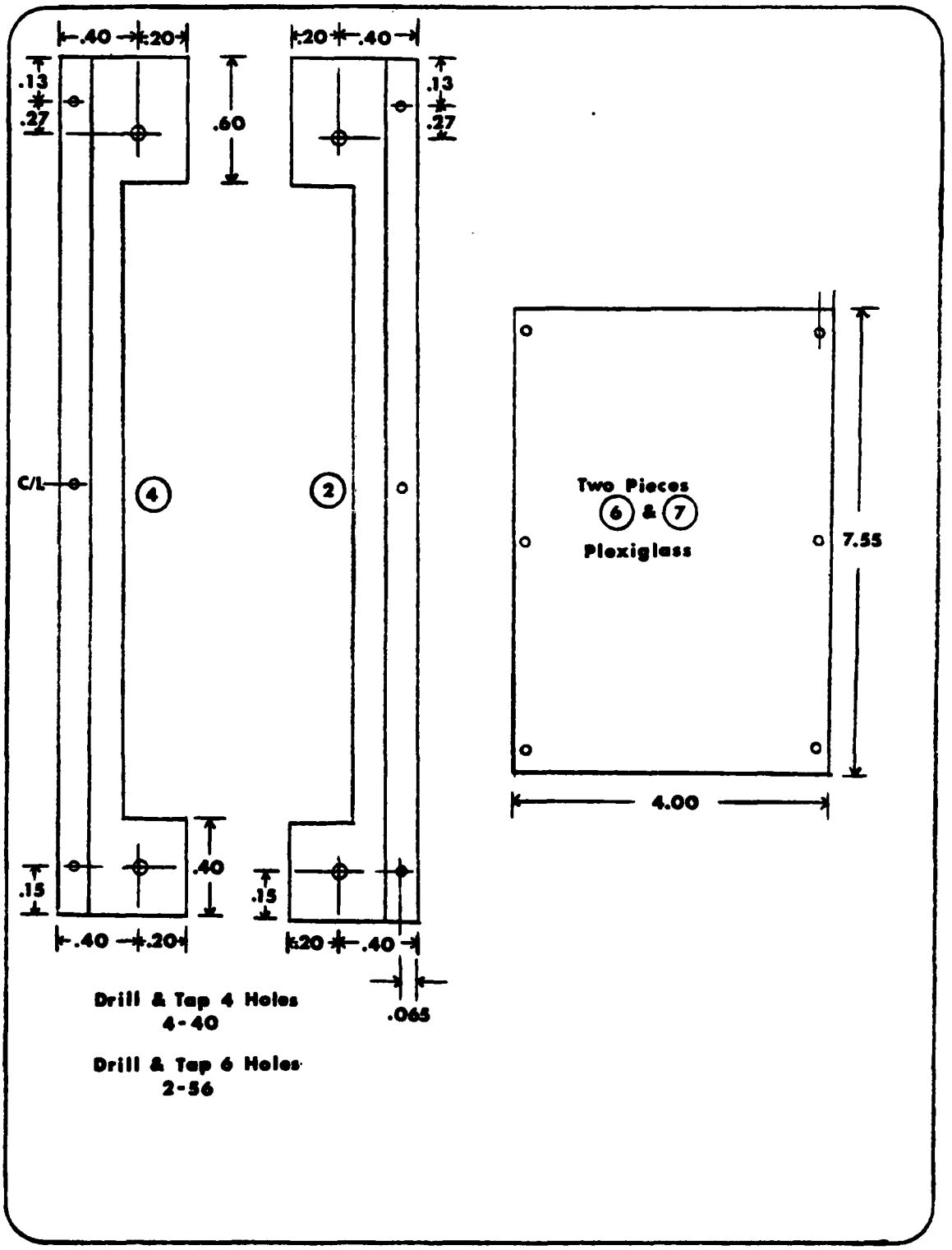
Appendix D: Frequency Shift Data

Phase Shifter Input (d.c Volts)	Thermometer Loop Frequency (MHz)	Clock Loop Frequency (MHz)
0.465	309.5935	298.6615
0.836	309.5916	298.6672
1.572	309.5894	298.6829
2.12	309.5885	298.6959
2.57	309.5883	298.7059
3.93	309.5877	298.7863
4.63	309.5872	298.7498
5.04	309.5871	298.7559
5.67	309.5863	298.7655
5.90	309.5860	298.7685
6.72	309.5859	298.7785
8.83	309.5860	298.8025
9.53	309.5862	298.8075
10.93	309.5865	298.8167
13.82	309.5872	298.8312
13.98	309.5872	298.8318
14.90	309.5874	298.8356
15.17	309.5877	298.8366
17.29	309.5884	298.8441
18.06	309.5882	298.8466
19.12	309.5883	298.8497
19.40	309.5909	298.8505
20.8	309.5885	298.8542
23.4	309.5911	298.8603
23.6	309.5911	298.8606
27.9	309.5918	298.8688
30.0	309.5917	298.8721
30.1	309.5918	298.8722

Appendix E: Package Diagrams




Outside View
Top View
3
.60
.50
1.17
1.13
.60
1.00
Top View
4
.13
.47
.40
6.29
.60
1.17
1
Front View
.39
.47
.14
.39
Dia. #33
.18
.18
Dia. #33
.18
.18
1.00
3
Outside View
2.00
Dia. #33
.18
.18
.39
Dia. #33
.18
.18
1.00
4
Drill & Tap Both Ends
4-40
2
.18
.18
.18
.18


.40
.20
.20
.40
.13
.27
.13
.27
.60
C/L
4
2
.40
.15
.15
.40
.20
.20
.40
.065
Drill & Tap 4 Holes
4-40
Drill & Tap 6 Holes
2-56
Two Pieces
6 & 7
Plexiglass
7.55
4.00

Vita

Jerry W. McGuire was born on 31 December 1946 in Roanoke, Virginia. He graduated from high school in Rocky Mount, Virginia in 1965 and entered the USAF in July, 1966. After serving an initial 4 year tour with the 49th Tactical Fighter Wing as a jet engine mechanic at Spangdahlem AB, Germany and Holloman AFB, New Mexico, he separated from the USAF. In 1970, he was employed by the General Electric Company in Salem, Virginia as an electronics technician while attending school part time. He received a Bachelor of Science degree in Electrical Engineering Technology from Virginia Polytechnic Institute in 1978, and re-entered the USAF through the OTS commissioning program. He then served as an Inertial Navigation System Components Analyst with the 6585th Test Group at Holloman AFB, New Mexico until entering the School of Engineering, Air Force Institute of Technology, in March 1982.

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A circuit, using standard "off-the-shelf" components, for digital temperature compensation of a SAW oscillator was designed. This circuit was implemented on a single circuit board. A crucial component of the circuit, the AFIT IC, designed by four previous AFIT students and fabricated by NCR, failed to operate at a required frequency of 37 MHz. This caused an early halt to the project; however, several parts of the design were tested individually with good results.

The portion of the circuit consisting of the D/A converter, op amp, and phase shifter was tested. For various addresses programmed on the D/A converter inputs, which simulated the output from the two EPROMs, a total phase shift of 107 degrees was obtained from the phase shift circuit. (Continued on reverse)

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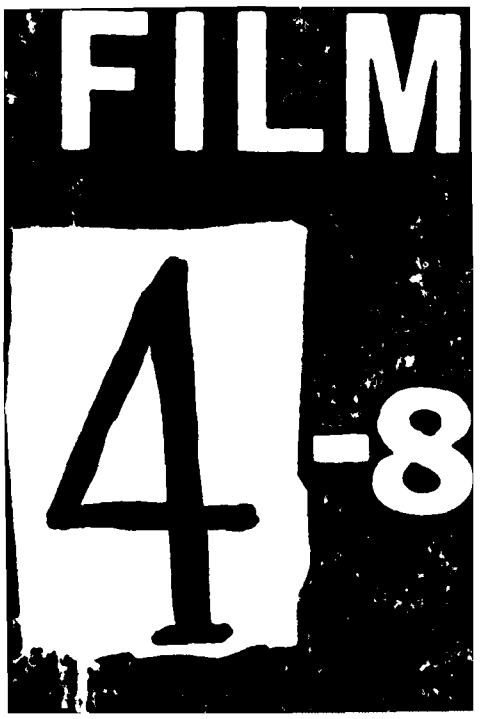
(Continued from Block 19)

The thermometer and clock paths of the SAW device were made to oscillate at their respective resonant frequencies by introducing the proper amounts of phase shift and attenuation into the feedback loops. The thermometer and clock resonant frequencies were 309 MHz and 298 MHz respectively.

Testing of the SAW feedback loops in conjunction with the phase shifter circuit showed the clock loop frequency could be varied over a range of 210.7 KHz. The thermometer loop frequency had a slight variation of 7.6 KHz. Finally, the SAW clock loop produced an output power of +9 dBm.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